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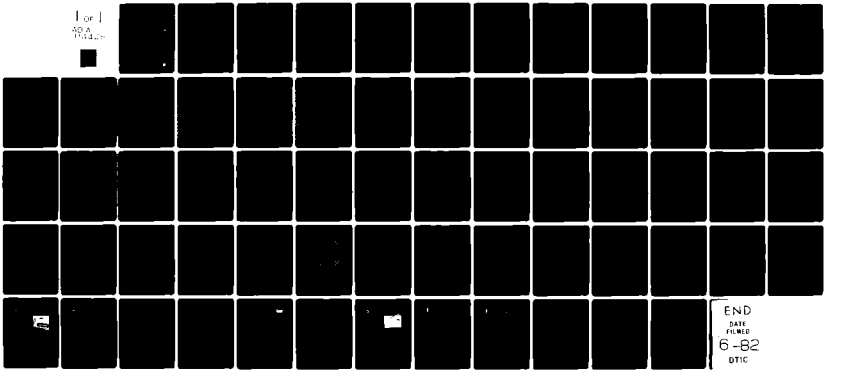

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HYDRAULIC UNIVERSAL DISPLAY PROCESSOR SYSTEM (HUDPS)

Grumman Aerospace Corporation
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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This six month study effort explored methods of display fault indication to ground support personnel and optimize microprocession circuitry for universal aircraft application.

Task I established the maximum number of sensors required for a complex, comprehensive diagnostic system for the F14A as 150: Inputs could be either analog or digital. For comparison purposes, an A6E system was considered.

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- Fault display methods were investigated with emphasis on smart alphanumeric devices in Task II. Volatile and non-volatile memory components were utilized along with the Intel 8748 microprocessor and associated EPROMS. The use of National Semiconductor ADC0816 data acquisition chips consisting of a 16 input multiplexer, an 8 bit A/D converter and an 8 bit tri-state buffered output facilitates the many inputs.
- Power consumption for a complete system was estimated as 5 watts while airborne. On the ground, 15 watts at 5 volts is required for display requirements.
- Display envelope would measure 8x7x6 and would contain approximately 6 circuit boards.

In Task III a universal display processor system was formulated. A Block Diagram and several flow diagrams were generated. Multiplexer schematics were established for analog and discrete inputs. An electrical component parts list was generated for a typical system.

PREFACE

This report was prepared by the Grumman Aerospace Corporation under Naval Air Development Center Contract Number N62269-81-C-0243 entitled "Display/Processor Fault Indication System".

The program was based on previous feasibility, development, and flight tests conducted and reported in the following published documents:

NADC Report No. TR75168-30 Final Engineering Report - Phase I - HYCOS

NADC Report No. TR76389-30 Hydraulic Diagnostic Monitoring System (Interim Report)

NADC Report No. TR76390-30 Hydraulic Diagnostic Monitoring System (Final Report)

This work task explored methods of display fault indications to ground support personnel and optimized microprocessor circuitry to allow use by any Navy aircraft.

The Display Processor System was designed for universal application to any Navy aircraft hydraulic system. A change in microprocessor programming compensates for hydraulic system differences and sensor variation requirements.

The sponsoring agency is the Naval Air Systems Command, Washington, D.C.

Mr. Steve Hurst - AIR340C was the Program Manager. Mr. Douglas O. Bagwell of NADC administered and provided technical guidance for this effort.

Grumman Aerospace Program Manager was Mr. Edwin A. Anderson with Mr. John J. Duzich and Herman L. Dreksler as Project Engineers.

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1 - SUMMARY

1.1 TASK I

The Task I effort established the maximum number of analog and digital sensors required for a comprehensive, complex diagnostic system for the F-14A aircraft as 150. The system, however, could handle up to 240 inputs. In addition, the A-6E INTRUDER system was used as a comparative aircraft for universal application.

Block diagrams of both the F-14A and A-6E were studied and are included in the report.

A brief description and listing of the display/processor fault indication system sensors was tabulated based on the F-14A vehicle. Supplementary display and action descriptors were generated to define and direct the course of action required as diagnosed by the system.

1.2 TASK II

Fault display methods for ground support personnel were investigated during Phase II with emphasis on smart alphanumeric devices. Electronics which convert ASCII data to alphanumerics was selected.

Both volatile and nonvolatile memory components are utilized in conjunction with the Intel 8751 microprocessor and the Intel 2764 and 2716 EPROMS. In addition, analog-to-digital conversions utilize a National Semiconductor ADC 0816 data acquisition chip consisting of a 16-input multiplexer, an 8-bit A/D converter, and an 8-bit tri-state buffered output.

Power and voltage requirements were investigated. Power consumption for a complete system is estimated at 5 W using a DC-to-DC converter for 28- to 5-volt conversion while the vehicle is airborne.

On the ground, 15 W is required during interrogation due to the display requirements.

The estimated display envelope is 8 x 7 x 6 in. and contains 30 ICs mounted on six circuit boards.

1.3 TASK III

In Task III, a universal hydraulic advanced display processor system was formulated for application to any aircraft hydraulic system. Input signals such as discrete voltages, analog voltage levels, and variable-frequency pulse trains are sampled, compared to a known valve, and stored in a nonvolatile memory. Different signal types are fed into separate multiplexers whose outputs are controlled by the microprocessor.

A typical block diagram and several flow diagrams were formulated. A sample program was then generated. Multiplexer schematics for both analog and discrete inputs were established.

Six different types of display technologies were investigated utilizing information from 54 manufacturers. An electrical component parts list was generated for a typical system. A detailed description of the recommended elements is included in this report.

2 - INTRODUCTION

The purpose of this Hydraulic Universal Display Processor System (HUDPS) study was to explore methods of display fault indications to ground support personnel for various aircraft hydraulic systems.

The study display/processor system covered a universal system capable of interfacing with any Navy aircraft hydraulic system by a change in software/microprocessor programming.

A systems approach was used for this study.

2.1 DIAGNOSTIC SYSTEM SIZE

In determining the largest, most complex processor required, Grumman Aerospace has selected the F-14 Tomcat because of its sophisticated multiple hydraulic systems. A hydraulic block diagram, Fig. 2-1, depicts the many subsystems used on the aircraft (Ref. 1). In addition, Fig 2-2 and 2-3 show details of the flight and combined power systems. For comparison, Fig. 2-4 illustrates the simplified Grumman A-6A hydraulic schematic.

The maximum number of sensors that might be used in an F14A hydraulic system is approximately 150 and are listed in Table 2-1. To a great extent, many of these sensors may be combined and optimized due to system requirements. The sensors used in the system are:

- Discrete (manually resettable)
- Reliable
- Self-checking (where possible)
- Analog
- Digital
- Non-intrusive (malfunction does not affect system operation).

For display purposes, a terminology list and action descriptors are listed in Table 2-2. This list does not include such items as corrective action and possible replacement part numbers.

2.2 FAULT INDICATION SYSTEM SENSORS

The hydraulic subsystem and major components dictate the maximum number of potential sensors required for an F-14 hydraulic system. The sensors would preferably be digital in nature. However, the universal system could handle analog and discrete inputs as well.

2.3 FAULT DISPLAY DESCRIPTORS

A study was performed to define the various component designations used throughout the vehicle with the resulting abbreviated display callout. This listing is presented in Table 2-2.

In conjunction with this listing, another tabulation defines the nature or severity of the problem based on sensor inputs. As a result of the combined lists, the:

- Nature
- Effect
- Location
- Remedial Action

would be sequentially displayed on the viewing panel.

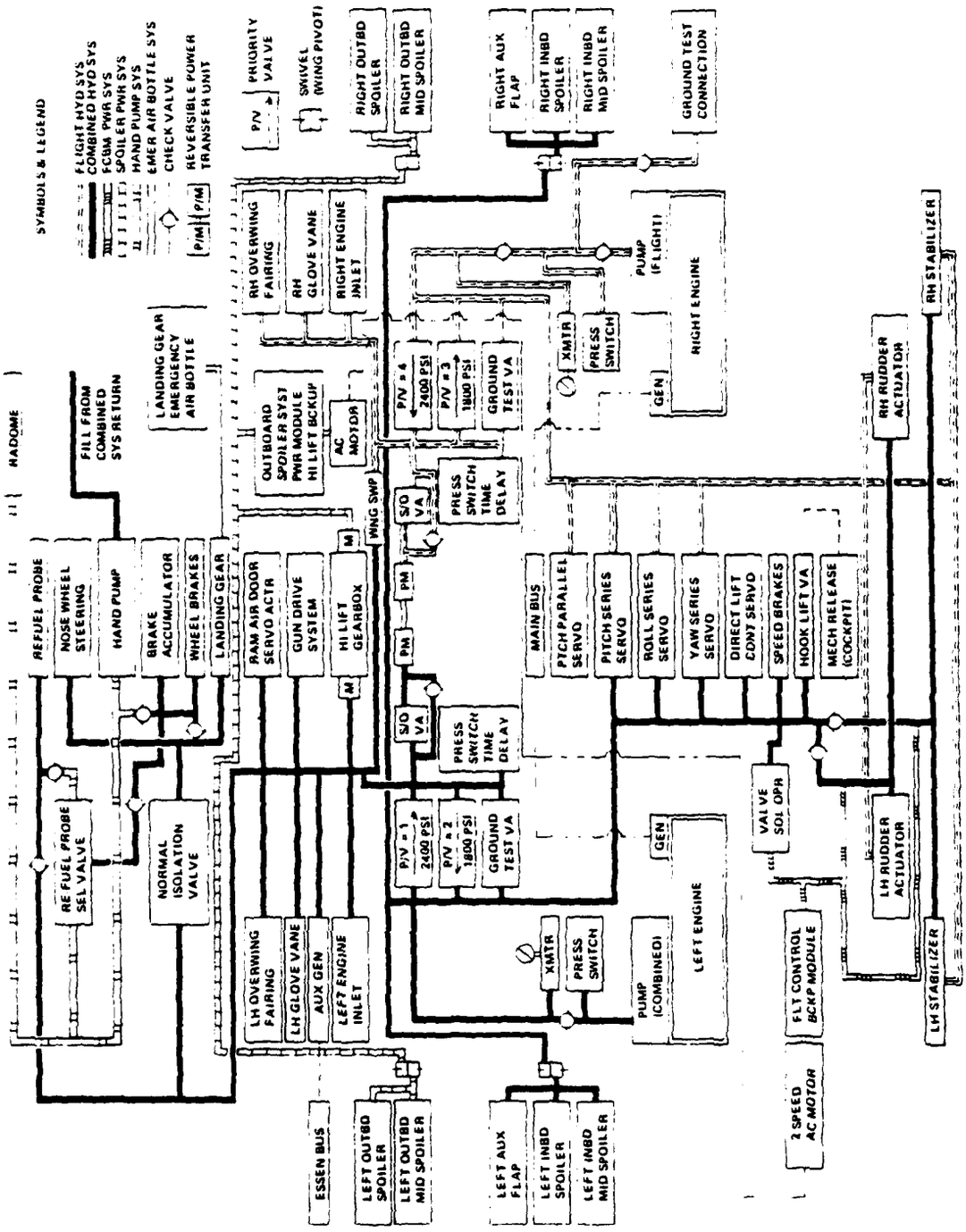
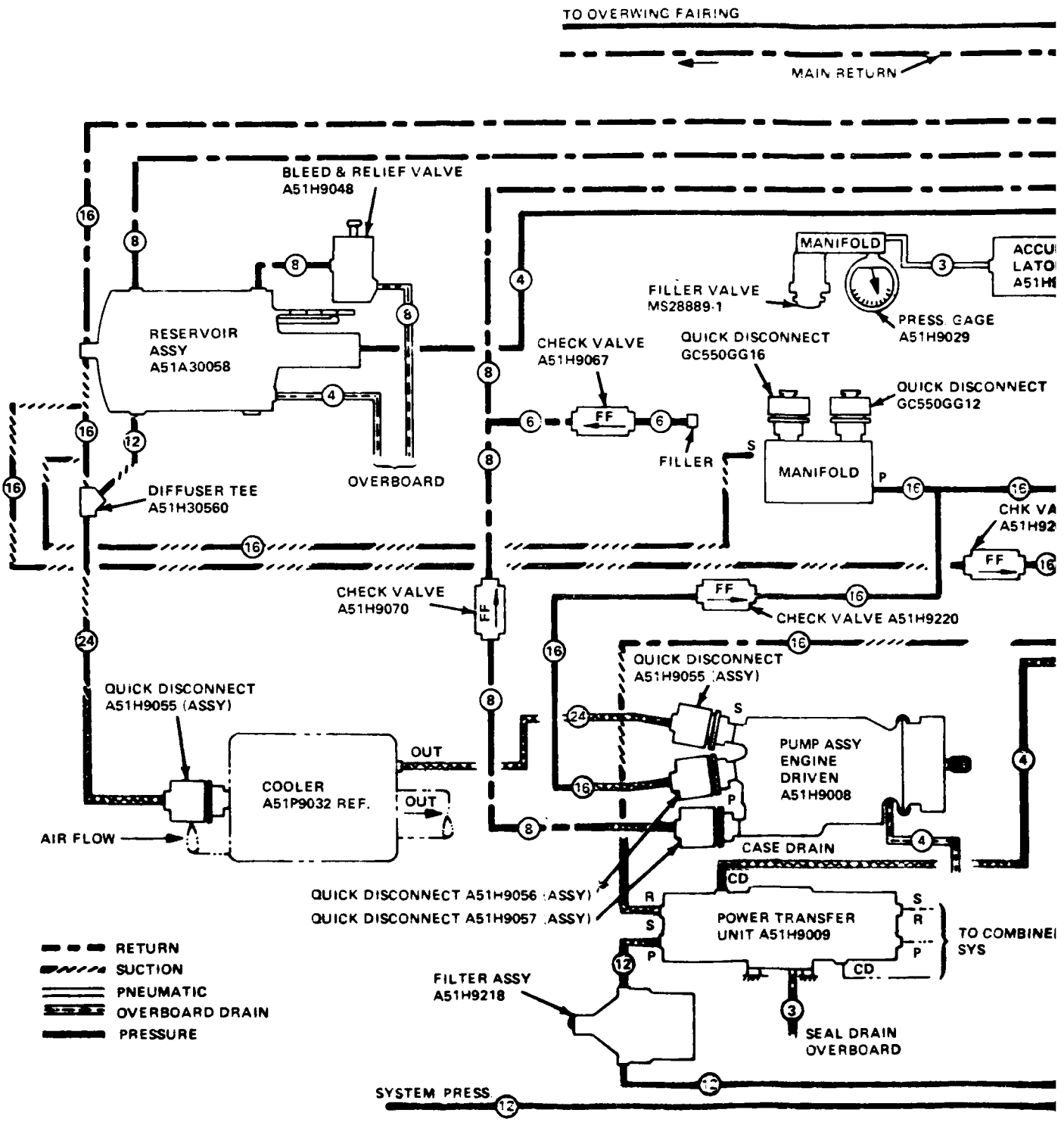


Fig. 2-1 F-14A Hydraulic System



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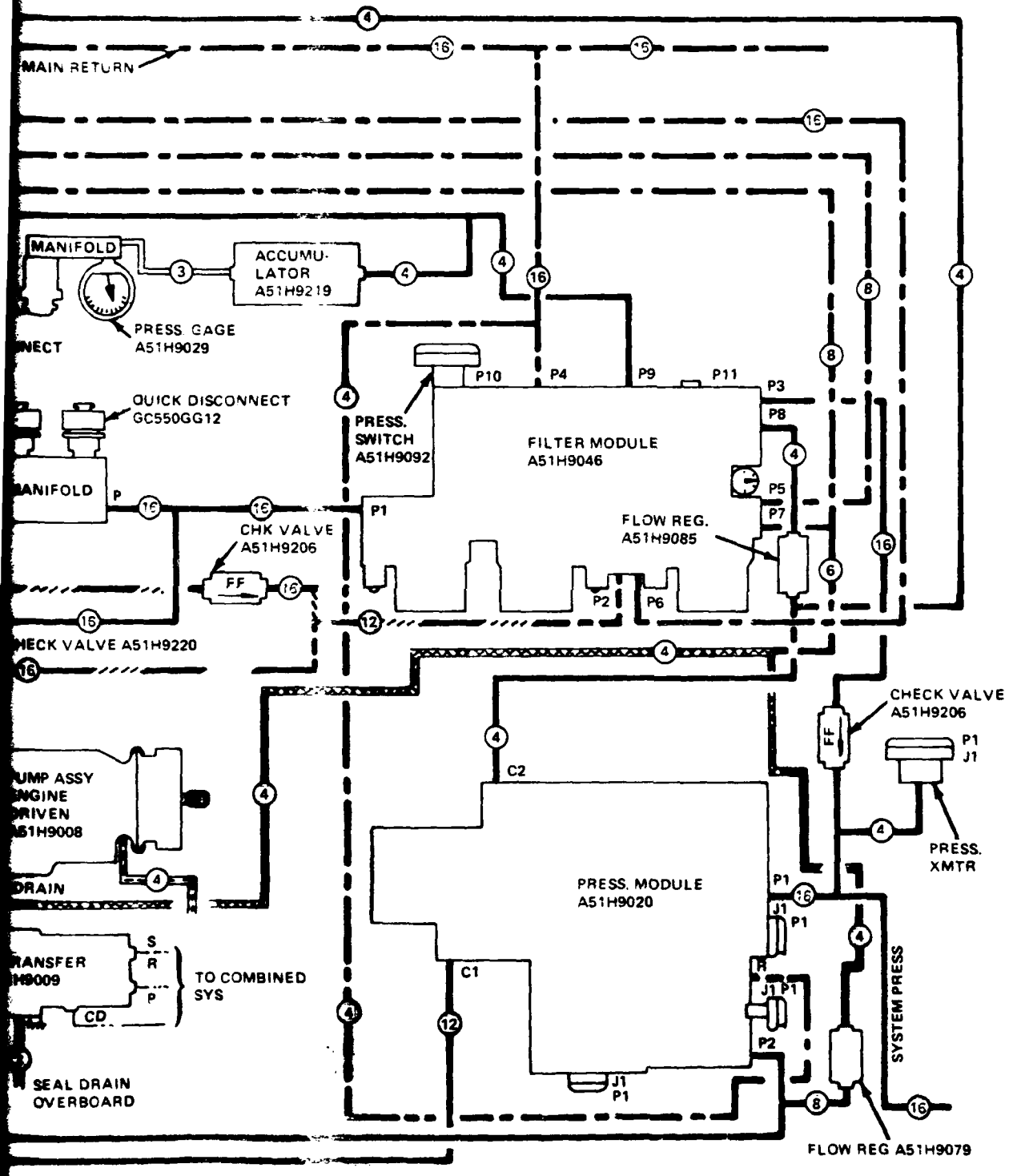
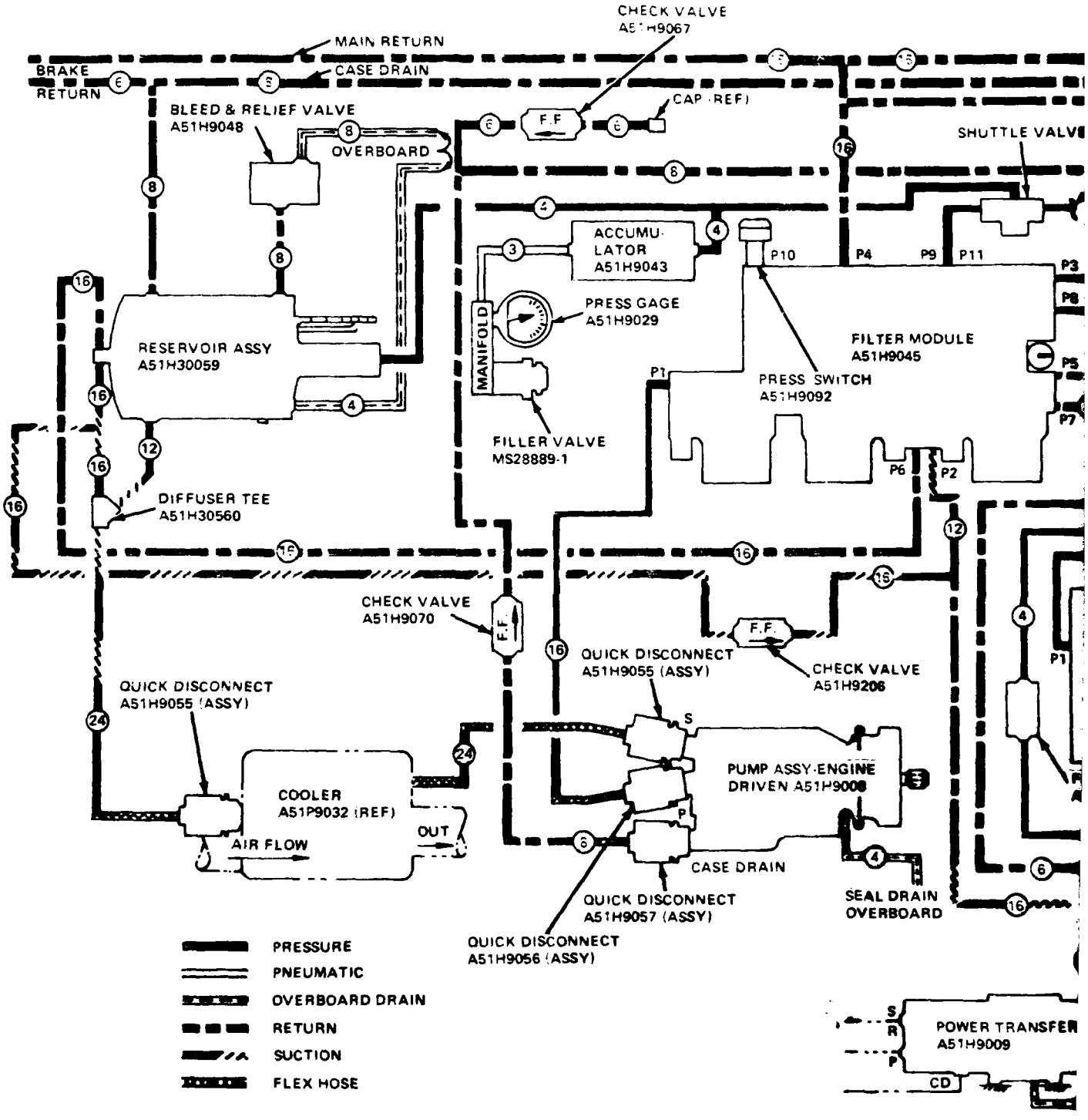


Fig. 2-2 Flight Power System



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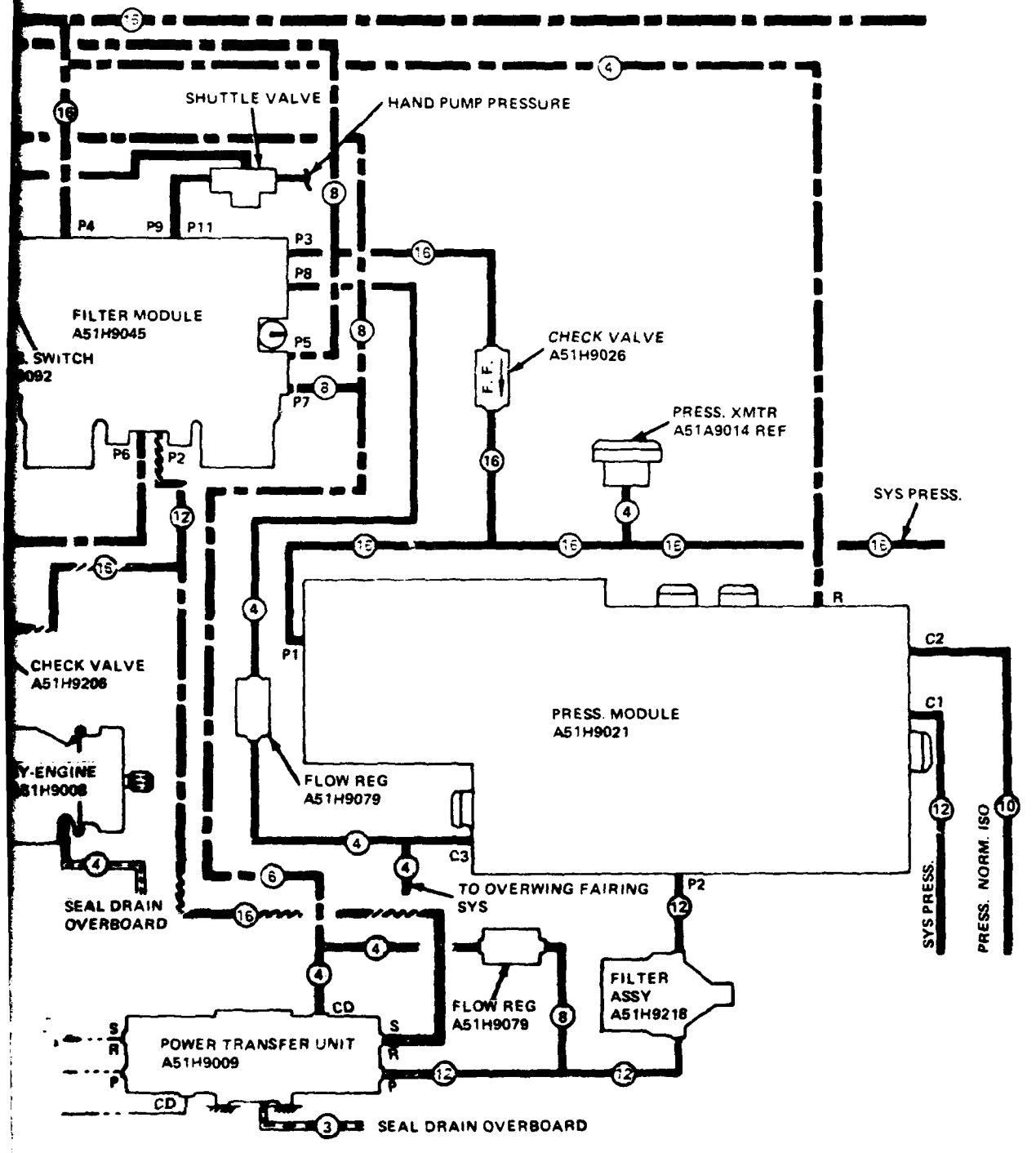

Fig. 2-3 Combined Power System

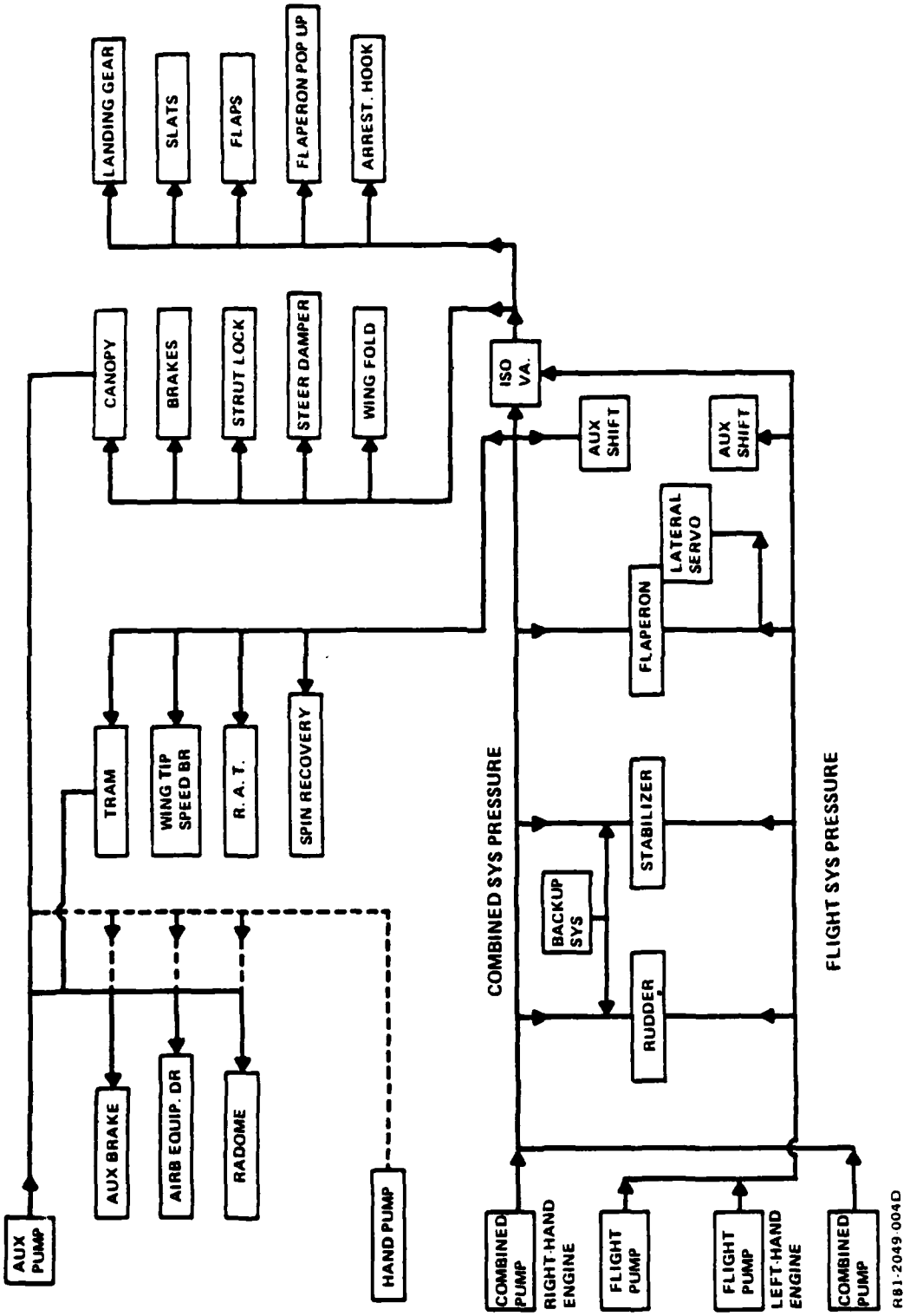

Fig. 2-4 A-6A Hydraulic Schematic

TABLE 2-1 DISPLAY PROCESSOR FAULT INDICATION SYSTEM SENSORS (SHEET 1 OF 2)

SYSTEM	SENSORS
REFUEL PROBE	• PRESSURE • DIFFERENTIAL PRESSURE • TEMPERATURE • FLOW
GUN DRIVE	• PRESSURE • DIFFERENTIAL PRESSURE • TEMPERATURE • FLOW
NOSE GEAR ABORT	• PRESSURE • DIFFERENTIAL PRESSURE • FLOW
NOSE WHEEL STEERING	• PRESSURE • DIFFERENTIAL PRESSURE • TEMPERATURE • FLOW
GLOVE VANE	• PRESSURE • DIFFERENTIAL PRESSURE • TEMPERATURE • FLOW • DIFFERENTIAL DISPLACEMENT
AICS	• PRESSURE • DIFFERENTIAL PRESSURE • TEMPERATURE • FLOW • DIFFERENTIAL DISPLACEMENT
EMERGENCY GENERATOR	• PRESSURE • DIFFERENTIAL PRESSURE • TEMPERATURE • FLOW
HI-LIFT CONTROL VA.	• PRESSURE • DIFFERENTIAL PRESSURE • TEMPERATURE • FLOW
MOTOR	• QUIESCENT FLOW
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SYSTEM	SENSORS
SPOILER MODULE	• PRESSURE • DIFFERENTIAL PRESSURE • TEMPERATURE • FLOW • LEVEL • DISPLACEMENT
MIDOUTBD/OUTBD SPOILERS	• PRESSURE • DIFFERENTIAL PRESSURE • TEMPERATURE • FLOW
WING SWEEP	• PRESSURE • DIFFERENTIAL PRESSURE • TEMPERATURE • FLOW • DIFFERENTIAL DISPLACEMENT
WHEEL BRAKE	• CONTINUITY • PRESSURE • DIFFERENTIAL PRESSURE • TEMPERATURE • PRECHARGE • FLOW • MOISTURE • BRAKE CLEARANCE
AUX FLAP	• PRESSURE • DIFFERENTIAL PRESSURE • TEMPERATURE • PRECHARGE • FLOW • MOISTURE
MIDINBD SPOILERS	• PRESSURE • DIFFERENTIAL PRESSURE • TEMPERATURE • FLOW
AFCS	• PRESSURE • DIFFERENTIAL PRESSURE • TEMPERATURE • QUIESCENT FLOW • FLOW • DIFFERENTIAL DISPLACEMENT

TABLE 2-1 DISPLAY PROCESSOR FAULT INDICATION SYSTEM SENSORS (SHEET 2 OF 2)

SYSTEM	SENSOR
SPEED BRAKE	• PRESSURE • DIFFERENTIAL PRESSURE • TEMPERATURE • FLOW
ARRESTING HOOK	• PRESSURE • DIFFERENTIAL PRESSURE • TEMPERATURE • FLOW
RUDDER/STABILIZER	• PRESSURE • DIFFERENTIAL PRESSURE • TEMPERATURE • QUIESCENT FLOW • FLOW • DIFFERENTIAL DISPLACEMENT
FCBM	• PRESSURE • DIFFERENTIAL PRESSURE • TEMPERATURE • FLOW • LEVEL • DISPLACEMENT
MAIN LANDING GEAR (6) - DOOR ACT. - INBOARD - OUTBOARD DOOR LOCK - TIMER VALVE	• PRESSURE • DIFFERENTIAL PRESSURE • TEMPERATURE • FLOW
NOSE LANDING GEAR	• PRESSURE • DIFFERENTIAL PRESSURE • TEMPERATURE • FLOW
OVERWING FAIRING	• PRESSURE • TEMPERATURE • FLOW
POWER TRANSFER UNIT	• CASE • FLOW • PRESSURE • TEMPERATURE
R81-2049-005(2/2)D	

SYSTEM	SENSORS
ACCUMULATORS BRAKE	• PRECHARGES • TEMPERATURE • DISPLACEMENT
- FLT	• PRECHARGE • TEMPERATURE • DISPLACEMENT
- COMB	• PRECHARGE • TEMPERATURE • DISPLACEMENT
- OVER WING FAIRINGS (2)	• PRECHARGE • TEMPERATURE • DISPLACEMENT
PNEUMATIC BOTTLES - CANOPY	• PRESSURE • TEMPERATURE • LIQUID
- LANDING GEAR	• PRESSURE • TEMPERATURE • LIQUID
- RAMP ACTUATORS	
PUMP	• FLOW • TEMPERATURE • PRESSURE • QUIESCENT FLOW • RPM • TORQUE
FILTERS	• PRESSURE • DIFFERENTIAL PRESSURE • TEMPERATURE • FLOW
RESERVOIRS	• AIR • TEMPERATURE • PRESSURE • LEVEL • RATE

TABLE 2-2 FAULT DISPLAY DESCRIPTORS

TERMINOLOGY	DISPLAY
FLIGHT SYSTEM	FLT SYS
COMBINED SYS	COMB SYS
FILTER	FILTER
(FLIGHT, COMB, PRESSURE, RETURN, CASE)	
DIFFERENTIAL PRESSURE	DELTA P
FLOW	
TEMP	
ISOLATION VALVE	ISO VALVE
PUMP	PUMP
CASE FLOW	CASE FLO
QUIESCENT FLOW	QUIES FLO
RESERVOIR	RESERVOIR
LEVEL	LEVEL
AIR	AIR
PRESSURE	PRESSURE
LEAKAGE	LEAK
ACCUMULATOR	ACCUMULATOR
DISPLACEMENT	DISPLACEMENT
PRESSURE	PRESSURE
TEMPERATURE	TEMPERATURE
PNEUMATIC BOTTLE	PNEU BOTTLE
PRESSURE	PRESSURE
TEMPERATURE	TEMPERATURE
CANOPY	CANOPY
GEAR	GEAR
DOOR	DOOR
RELIEF VALVE	RELIEF VALVE
LEAKAGE	LEAK
SYSTEM	SYSTEM
PRESSURE	PRESSURE
TEMPERATURE	TEMPERATURE
FLIGHT CONTROL BACKUP	FCBM
TEMPERATURE	TEMPERATURE
LEVEL	LEVEL
SHOCK STRUTS	SHOCK STRUTS
PRESSURE	PRESS
LEVEL	LEVEL
DISPLACEMENT	DISPLACEMENT
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TERMINOLOGY	DISPLAY
BRAKE	BRAKE
TEMP	TEMP
PAD WEAR	DISC PADS
FLUID LEVEL	LEVEL
ACCUM PRESS	ACCUM PRESSURE
MOISTURE	WATER
ELAPSED TIME	ELT
FLIGHT DURATION	FLT DUR
TAIL HOOK DASH POT	TAIL HOOK
PRESSURE	PRESSURE
TEMP	TEMP
RUDDER ACTUATOR	RUDDER
QUIESCENT FLOW	QUIES FLO
STABILIZER ACTUATOR	STAB
QUIESCENT FLOW	QUIES FLO
TRANSFER PUMP	TRANS PUMP
FLOW	FLOW
TEMPERATURE	TEMPERATURE
SPOILER PACKAGE	SPOILER
3 ϕ WINDINGS	PRESSURE
(PHASE OPERATION	TEMPERATURE
	PHASE
	OPEN CIRCUIT
CAVITATION	CAVITATION

ACTION DESCRIPTORS	
REPLACE	OVERHEAT
SERVICE	OVERTEMPERATURE
HIGH	FILTER CLOGGED
LOW	SENSOR DEFECTIVE
INDICATOR	MAINTENANCE REQUIRED
INOPERATIVE	SYSTEMS GO
ADJUST	IMPENDING FAILURE
ALIGN	EMERGENCY CONDITIONS
SECURE	PUMP WEAR
LEAKAGE	FLUID CONTAMINATED
	PUMP INOPERATIVE
	PUMP ISOLATED
	SYS A ISOLATED

3 - DISCUSSION

3.1 GENERAL CONSIDERATIONS

Methods of display fault indication for ground support personnel have been investigated with emphasis on "smart" alphanumeric devices. The "smart" portion of the display contains the electronics that converts ASCII data to alphanumerics, refreshes the display so that it is flicker-free, and has the knowledge of where to put each character in the display. These "smarts" should be purchased from the display manufacturer with the display itself using their existing pre-programmed microcomputer circuitry, as it is reasonably priced and requires no additional design. A recommended example is the Hewlett-Packard HDSP-2471 used in conjunction with their HSDP-2432, which is a 32-character alphanumeric display panel using LEDs organized in a 5x7 dot matrix.

The overall electronic system including the display, microprocessor, support circuits, and analog/digital requirements have been studied and an electronic system is proposed that is adaptable to any Navy aircraft by using removable firmware program modules. Memory requirements, both volatile and nonvolatile, have been included to ensure handling the most complex system. The recommended microprocessor for system control is the Intel 8751 operating with Intel 2764 and 2716 Eraseable Programmable Read Only Memories (EPROMs). Analog-to-digital (A/D) conversion is done under microprocessor control using National Semiconductor ADC 0816 data acquisition chips that consist of a 16-input multiplexer, an 8-bit A/D converter, and an 8-bit tri-state output. Inputting digital data is done using TTL multiplexer ICs with an eventual tri-state output. The tri-state output allows many data outputs to be tied to a common data bus without loading. A system block diagram with a description of operation is included in this report.

Power and voltage requirements have been kept to a minimum. The power estimate for the complete system will be approximately 5 W using a DC-to-DC converter to change the aircraft 28 V to 5 V while the box is airborne, and 15 W using a 5-V at 5-A DC power supply while the unit is being interrogated on the ground.

A parts list listing the number of parts and the box size is included. The estimate is for 30 ICs mounted on six circuit boards plugged into a box that measures 8 x 7 x 6 in.

Flow diagrams for airborne and ground-based operations have been generated. A typical microprocessor program for a very basic system has been generated and is also included. Typical schematics of the multiplexing schemes for analog and digital inputs are shown and described.

A study of display technologies and methods of character generation has been completed with the results presented.

3.2 HUDPS BLOCK DIAGRAM DESCRIPTION

The Hydraulic Universal Display Processor System (HUDPS) is a display/processor system designed for universal application to any aircraft hydraulic system. Hydraulic signals in the form of discrete voltages, analog voltage levels, and variable-frequency pulse trains are sampled, compared to a known value, and stored in a non-volatile memory as a "1" for a failure or a "0" for no failure. There is also a provision for driving outputs to help overcome failures (control function).

Figure 3-1 shows the HUDPS block diagram. Each of the different types of signal are fed into separate multiplexers whose outputs are controlled by the microprocessor (MP).

Discrete inputs are digital-level signals and require no signal processing. Analog signals are converted to digital equivalents with the MP controlling the analog-to-digital (A/D) converter. The variable-frequency pulses are outputs of a voltage-to-frequency (V/F) converter which are fed into a counter for a unit time; the

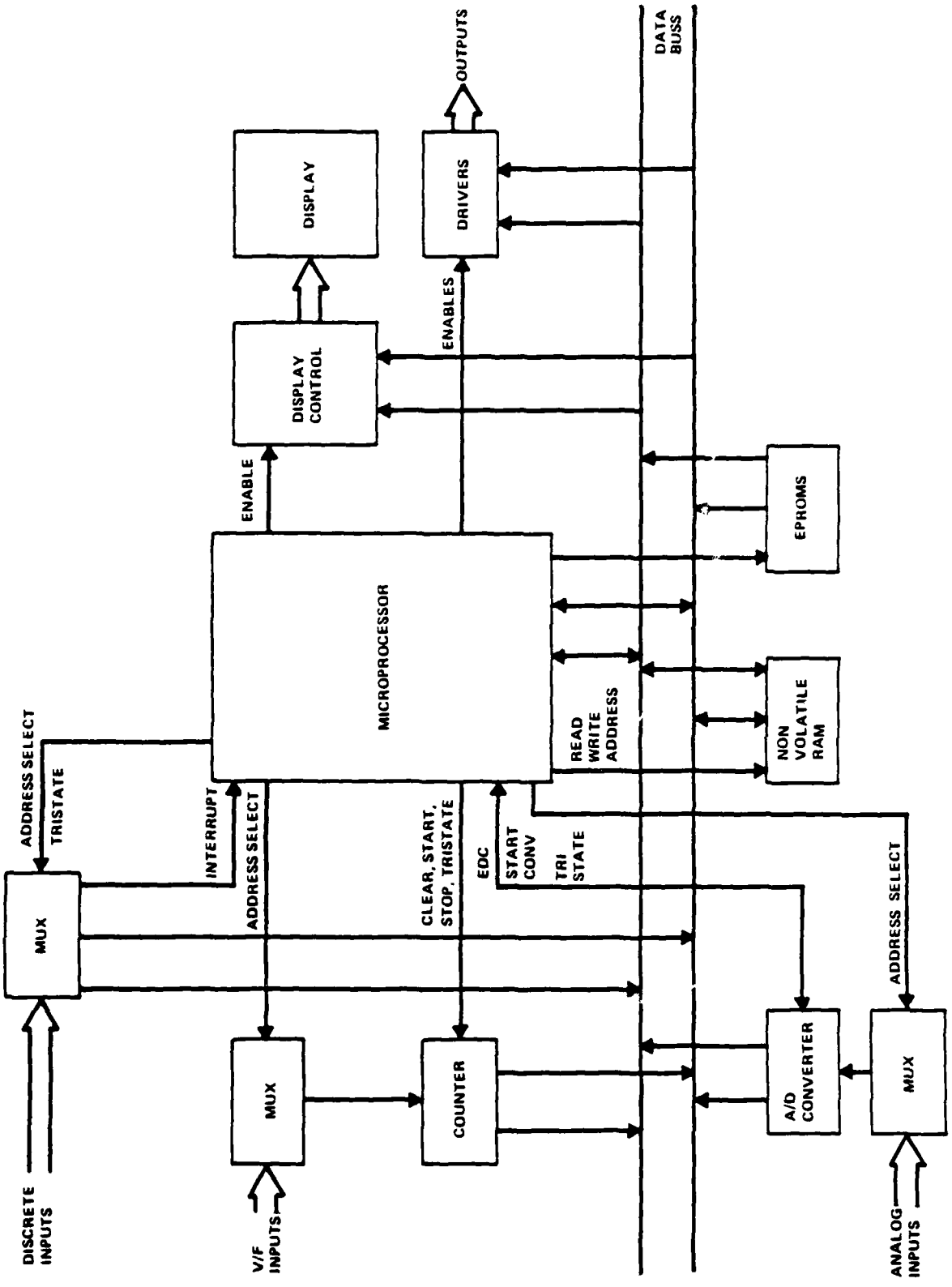


Fig. 3-1 HUDPS Block Diagram

result is that an initial analog voltage has now been converted to its digital equivalent.

The MP addresses each of the multiplexers and selects one signal to be operated on at a time. For the discretes, the MP steps through the individual signals one at a time and enables the discrete multiplexer to feed the data bus. The MP inputs the data from the bus and operates on it.

For the V/F inputs the MP selects one input, clears a counter, enables the digital data to load the counter for a predetermined unit time, and then inhibits further data from entering the counter. The data is then loaded onto the data bus and acquired by and operated on by the MP.

One analog data channel at a time is MP selected and directed through the multiplexer into the A/D converter which starts conversion when commanded to by the MP; upon completion, the A/D converter sends out an end of conversion (EOC) signal. The data is then available to the data bus and is acquired by and operated on by the MP.

Failure information is stored in the nonvolatile RAM (NOVRAM). The MP determines whether the NOVRAM reads or writes data and to or from what address. Data is transferred between the MP and the NOVRAM across the data bus.

If an in-flight failure occurs that can be corrected by electronic action, the MP controls drivers that accept information from the data bus to perform the corrective action(s). The corrective action(s) are preprogrammed in the PROM, which is a 28-pin integrated circuit (0.6 in. wide by 1.4 in. long) that can be removed from its socket and replaced by one with a different program for different corrective actions (such as for different aircraft types).

For display circuitry operation, the MP sequences throught the NOVRAM memory looking for failures. A failure indication and its particular address signals the MP where to go in the data PROM to acquire data associated with that failure. The

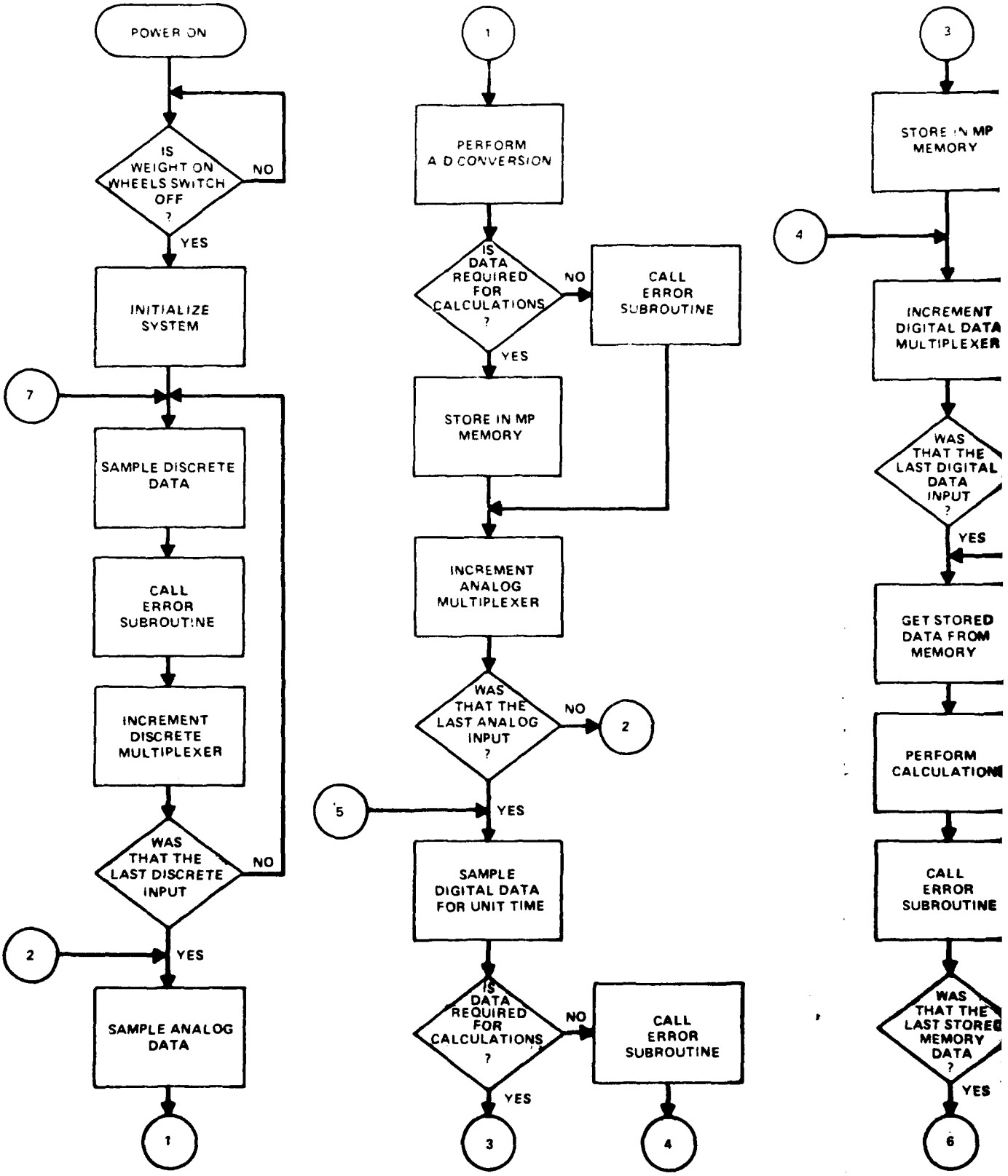
MP feeds the data to be displayed to the Display Control circuitry. The latter is a "smart" system that decodes ASCII data, positions the data on the readout, refreshes the data to avoid flicker, and holds the data until told to change. The display is comprised of alphanumeric characters.

3.3 FLIGHT EXECUTIVE FLOW DIAGRAM

The flight executive flow diagram is shown in Fig. 3-2. During this routine, each data line is sampled one at a time. Discretes are checked for either a "1" or "0"; analog data is converted to digital and either compared to a preset value or stored if it is required for a later calculation. Digital data (from V/F converters) is counted for a unit time and compared to a preset value, or stored if it is required for calculations. After all inputs have been sampled, the data stored in memory for calculations are acted on. Errors are stored in the NOVRAM RAM. At the end of the flight the RAM data is transferred to the NOVRAM EEPROM.

The flow diagram description is as follows:

- Power is applied
- The unit waits until the weight on wheels switch is off, showing that the aircraft is airborne
- All internal registers, counters, memories, and control circuits are initialized
- The discrete data is sampled (Fig. 3-2, (7))
- The error subroutine is called (see error subroutine)
- The multiplexer is incremented to sample the next data input
- If more discrete data must be sampled, the program is returned to (7) above and the loop repeated. The loop from (7) is repeated until all of the discretes have been checked
- The analog data is sampled (Fig. 3-2, (2))
- A/D conversion is performed



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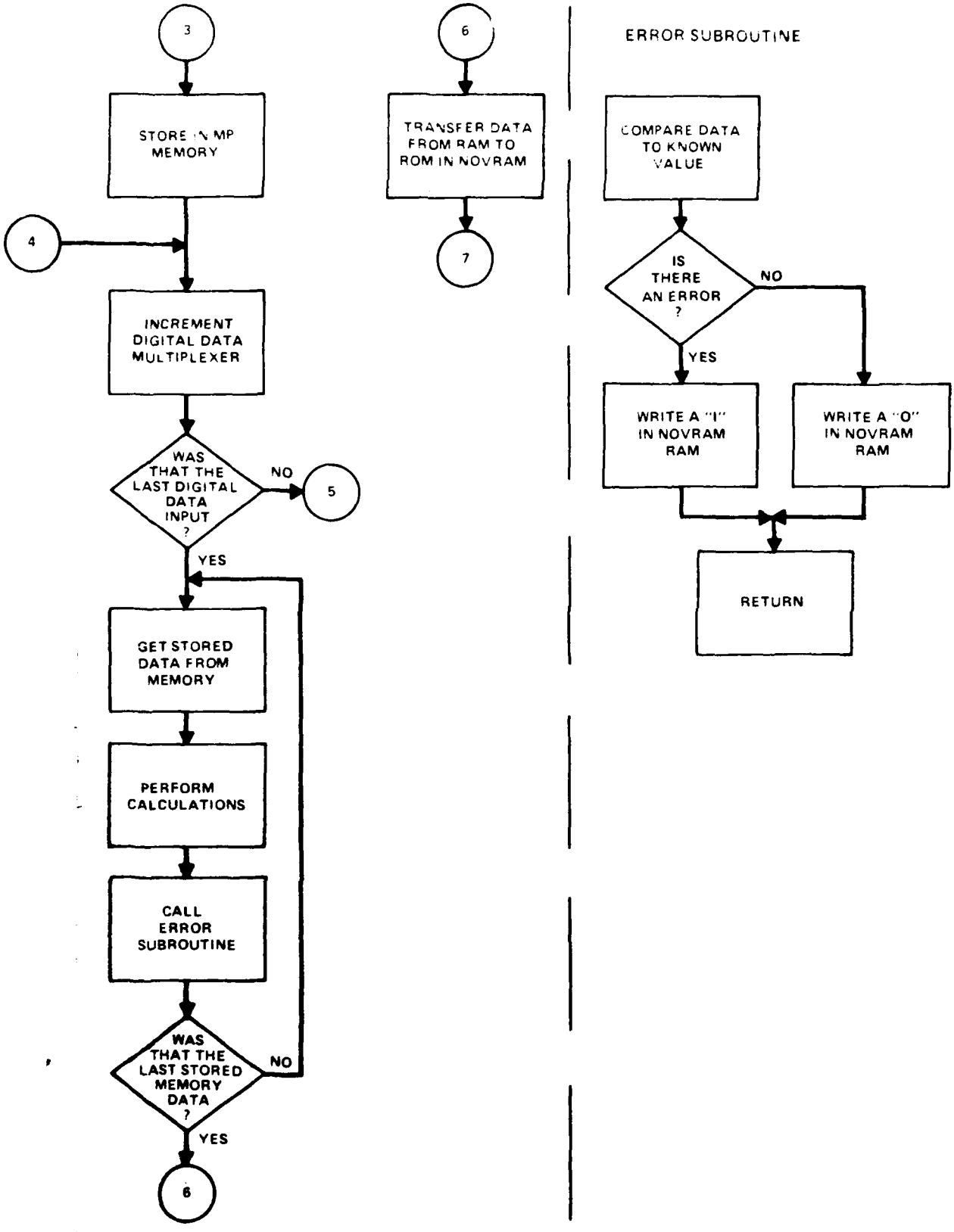

Fig. 3-2 Flight "Executive" Flow Diagram

3.4 FLOW DIAGRAM: ERROR SUBROUTINE

The error subroutine included in Fig. 3-2 checks that the data is correct. If there is an error, a "1" is written into the NOVRAM RAM at a known address (for no error, a "0" is written). After writing, the program returns to the Executive Routine.

- If the data is not required for a later calculation, the error subroutine is called. If it is required for a later calculation, the data is stored in the microprocessor RAM for later use
- The analog multiplexer is incremented
- The loop from (2) above is repeated until all of the analog channels of data have been sampled
- A digital data channel is fed into a counter for a unit time. This data is derived from a voltage-to-frequency (V/F) converter (Fig 3-2, (5))
- If the data is not required for a later calculation, the error subroutine is called. Otherwise, the data is stored in the microprocessor RAM for later use
- The digital data multiplexer is incremented
- The loop from (5) above is repeated until all of the V/F channels have been sampled
- The data required for calculations are called from the RAM memory
- Calculations are performed
- The error subroutine is called
- Calculations continue until completed
- When this routine is completed, data are transferred from the RAM to the EEPROM in the NOVRAM.

3.5 FLOW DIAGRAM: GROUND EXECUTIVE ROUTINE

The executive flow diagram for the aircraft on the ground is shown in Fig. 3-3. This routine includes a self-test, an examination of the error memory for failures that have occurred in flight, and error results and actions to be taken using the alphanumeric display. The operation follows:

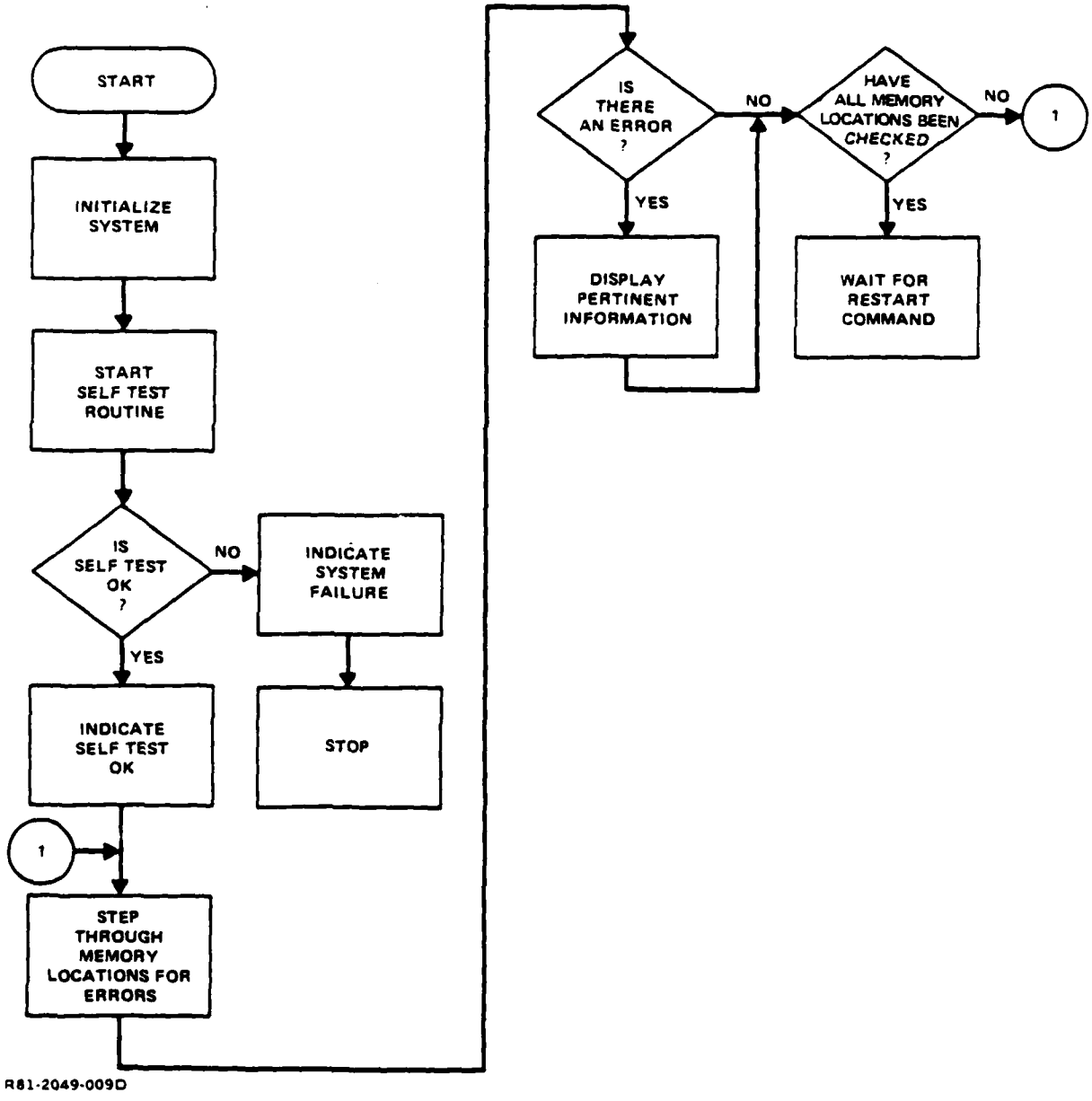

Fig. 3-3 Executive Program Flow Diagram (Ground)

- Power is applied to the system, an indication of being on the ground (such as the output of the weight on wheels switch), and a start command (possibly from a momentary switch) enables the system to start
- All counters, registers, and control states are initialized, and the NOVRAM/RAM is loaded with the data stored in its EEPROM.
- If self-test fails, a system failure will be indicated and the system will stop. If the self-test is correct, the display will indicate a self-test OK (Fig. 3-3, (1))
- Look for an error indication in the NOVRAM and increment the address counter. If there is an error, the pertinent information about the memory location is displayed (the type of failure, the location of the failed component, replacement part number). If there is no error, verify that all memory locations have been tested. If they haven't, return to item (1) above and repeat
- If all memory locations have been tested, stop and wait for a restart command.

3.6 MICROPROCESSOR PROGRAM

A simple program using an 8748 microprocessor has been written to interface with a Hewlett Packard smart display and two switches used to simulate system failures. The 8748 is the forerunner of the 8751 microprocessor, which is the recommended unit for ultimate system use. The 8748 has 1K bytes of EPROM, one timer, 64 bytes of RAM, and three 8-bit I/O ports.

The program, shown in Fig. 3-4, continuously samples the two switches to determine if there is a failure. If there is no failure, the words "*ALL SYSTEMS OPERATIONAL*" is printed out. The sentence is held for approximately 2 sec and the program again samples the two switches. Two randomly selected three-line messages were written into the microprocessor PROM to simulate actual conditions.

```
ASM48 V1V3 SRC TITLE('FDI 11/20/81') PRINT (LP:)


ISIS-II MCS-48/UPI-41 MACRO ASSEMBLER, V3.0            PAGE    1
FDI 11/20/81

  LOC  OBJ        LINE       SOURCE STATEMENT

  0000             1              ORG 0
  0000 0405        2              JMP EXEC        ;LEAVE 0 OPEN FOR INTERRUPT
  0002 00          3              NOP
  0003 00          4              NOP
  0004 00          5              NOP
  0005             6 EXEC         ORG 5
  0005 1465        7              CALL RESET
  0007 2220        8              MOV A,#20H
  0009 146E        9              CALL INPUT
  000B 22E7       10              MOV A,#0E7H     ;SEND OUT CONTPOL WORD
  000D 146E       11              CALL INPUT      ;BLOCK TRANSFER
  000F 22FF       12              MOV A,#0FFH     ;INITIALIZE P2 AS INPUT PORT
  0011 3A         13              OUTL P2,A
  0012 00         14              NOP
  0013 00         15              NOP
  0014 00         16 E1           IN A,P2
  0015 1217       17              JB0 EPPOP1      ;TEST EPPOP INPUTS
  0017 00         18 E2           IN A,P2
  0018 1241       19              JB1 EPPOP2
  001A 00         20              IN A,P2
  001B 1217       21              JB0 EPPOP1
  001D 1465       22              CALL RESET
  001F B800       23              MOV R0,#00H     ;SET DATA REGISTER AT LOCATION 00
  0021 1458       24              CALL WORD       ;TO OBTAIN DEFAULT DISPLAY
  0023 1469       25              CALL MS2000
  0025 0405       26              JMP EXEC
  0027 1465       27 EPPOP1       CALL RESET
  0029 5820       28              MOV R0,#20H
  002B 1458       29              CALL WORD
  002D 1469       30              CALL MS2000
  002F 1465       31              CALL RESET
  0031 5840       32              MOV R0,#40H
  0033 1458       33              CALL WORD
  0035 1469       34              CALL MS2000
  0037 1465       35              CALL RESET
  0039 5860       36              MOV R0,#60H
  003B 1458       37              CALL WORD
  003D 1469       38              CALL MS2000
  003F 0417       39              JMP E2
  0041 1465       40 EPPOP2       CALL RESET
  0043 5800       41              MOV R0,#00H     ;PRINT OUT MESSAGE FOR FILTER #2
  0045 1458       42              CALL WORD
  0047 1469       43              CALL MS2000
  0049 1465       44              CALL RESET
  004B B8A0       45              MOV R0,#0A0H
  004D 1458       46              CALL WORD
  004F 1469       47              CALL MS2000
  0051 1465       48              CALL RESET
  0053 B8C0       49              MOV R0,#0C0H
  0055 1458       50              CALL WORD
  0057 1469       51              CALL MS2000
  0059 0405       52              JMP EXEC
  005B BF20       53 WORD         MOV R7,#20H
  005D F8         54 INCR         MOV A,R0
R81-2049-025(1/3)D
```

Fig. 3-4 Sample Program (Sheet 1 of 3)

```
ISIS-II MCS-48 UPI-41 MACRO ASSEMBLER, V3.0          PAGE    2
FDI 11/20/81

  LOC  OBJ        LINE       SOURCE STATEMENT

  005E ED           55              MOVP3 A,@A
  005F 146E         56              CALL INPUT
  0061 1B           57              INC R3
  0062 EF50         58              DJNZ R7,INCR
  0064 83           59              RET
  0065 2301         60 RESET        MOV A,#01H
  0067 39           61              OUTL P1,A
  0068 1485         62              CALL MS500
  006A 2302         63              MOV A,#02H
  006C 39           64              OUTL P1,A
  006D 83           65              RET
  006E 82           66 INPUT        OUTL BUS,A
  006F 2302         67              MOV A,#02H
  0071 39           68              OUTL P1,A
  0072 17           69              INC A
  0073 39           70              OUTL P1,A
  0074 BA01         71              MOV R2,#01H
  0076 1479         72              CALL MS20
  0078 83           73              RET
  0079 2300         74 MS20         MOV A,#00H
  007B 62           75              MOV T,A
  007C 55           76              STRT T
  007D 1681         77 CONT         JTF DECR
  007F A47D         78              JMP CONT
  0081 55           79 DECR         STOP TCNT
  0082 EA79         80              DJNZ R2,MS20
  0084 83           81              RET
  0085 BA09         82 MS500        MOV R2,#9H
  0087 1479         83              CALL MS20
  0089 83           84              RET
  008A BAFF         85 MS2000       MOV R2,#0FFH
  008C 1479         86              CALL MS20
  008E 83           87              RET
  0100              88 DATA         ORG 100H
  0100 20202020     89              DB    'ALL SYSTEMS OPERATIONAL'
  0104 414C4C20
  0108 53595354
  010C 454D5320
  0110 4F504552
  0114 4154494F
  0118 4E414C20
  011C 20202020
  0120              90              ORG 120H
  0120 20525544     91              DB   'RUDDER CONTROL SYSTEM FAILURE'
  0124 44455220
  0128 434F4E54
  012C 524F4C20
  0130 53595354
  0134 45402046
  0138 41494C55
  013C 52452020
  0140              92              ORG 140H
  0140 434F4E54     93              DB  'CONTROL UNDER PILOT SEAT ON LEFT'
  0144 524F4C20
  0148 554E4445
R81-2049-025(2/3)O
```

Fig. 3-4 Sample Program (Sheet 2 of 3)

```
ISIS-II MCS-48/UPI-41 MACRO ASSEMBLER, V3.0          PAGE   3
FDI 11/20/81

  LOC  OBJ        LINE       SOURCE STATEMENT

  0340 52205049
  0350 4C4F5420
  0354 52454154
  0359 204F4E20
  0350 4C454654
  0360              94              ORG 160H
  0360 52455044     95              DB  'REPLACE WITH MRA ASSY 6823-22-19'
  0364 41434520
  0368 57495448
  036C 20575241
  0370 20415352
  0374 59204720
  0378 22222022
  037C 2222D122
  0380              96              ORG 180H
  0380 20204859     97              DB  '*HYDRAULIC FILTER #7 CLOGGED*'
  0384 44524155
  0388 4C494320
  038C 46494C54
  0390 45522023
  0394 2720434C
  0398 4F474745
  039C 442A2020
  03A0              98              ORG 1A0H
  03A0 20464954     99              DB  '*FILTER IN ENGINE COMPARTMENT*'
  03A4 54455220
  03A8 494E2045
  03AC 4E474494E
  03B0 45204346
  03B4 4D504152
  03B8 54404546
  03BC 542A2020
  03C0              100             ORG 1C0H
  03C0 20202052     101             DB    '*REPLACE WITH TYPE CC-07634*'
  03C4 45504C41
  03C8 43452057
  03CC 49544820
  03D0 54595045
  03D4 2043432D
  03D8 30373634
  03DC 342A2020
                    102             END

  USER SYMBOLS
  CONT   007D   DATA   000F   DECR   0001   E1     0014   E2     0017   ERROR1 0027   ERROR2 0041   EXEC   0005
  INCR   005D   INPUT  006E   M520   0079   M52000 000A   M5500  0005   RESET  0065   WORD   005B

  ASSEMBLY COMPLETE,  NO ERRORS
R81-2049-025(3/3)D
```

Fig. 3-4 Sample Program (Sheet 3 of 3)

These are shown on Page 2 of Fig. 3-4 starting at Line Number 91 and continuing until the end of the program on Page 3 (Line Number 102).

For the first type of error the display reads out:

"*RUDDER SWITCH NOT OPERATING*"	Holds for 2 sec
"*SWITCH IN LOWER LEVEL*"	Holds for 2 sec
"*SWITCH PART #M8805/99-010*"	Holds for 2 sec

The program then samples the next switch. If a failure occurs, its error message is printed out and the program then returns to the start of the program and repeats.

The program was written in assembly language shown in the column headed "Source Statement". An assembler translated this language to a hexidecimal code shown in the column headed "OBJ". The assembler also prints out a location in PROM of each line of data ("LOC") and a line number for convenience in trouble-shooting ("LINE").

3.7 ANALOG MULTIPLEXER SCHEMATIC

The schematic diagram of the Analog Multiplexer is presented in Fig. 3-5 and 3-6. This shows a total of 112 analog inputs controlled by one 8-bit port from the microprocessor (MP). Note that one of the ADC 0816s is not used, so that we can disconnect all of these devices from the microprocessor data bus with the input code $\overline{AD62} \bullet \overline{AD72} \bullet \overline{AD82}$. This is necessary to prevent lockup of the data bus by the analog inputs.

The ADC 0816 is a 16-input A/D converter and multiplexer with a tri-state output that allows the device to be tied to the data bus directly. Four input address lines (AD12, AD22, AD32, AD42) permit the selection of one of the 16 inputs through its multiplexer. The ALE input (Address Latch Enable) signal from the MP locks the address into the device. AD52 starts the A/D conversion within the block. After conversion, one combination of the three address bits (AD62, AD72, and AD82) enables eight outputs of one of the seven ADC0816s to feed the bus data.

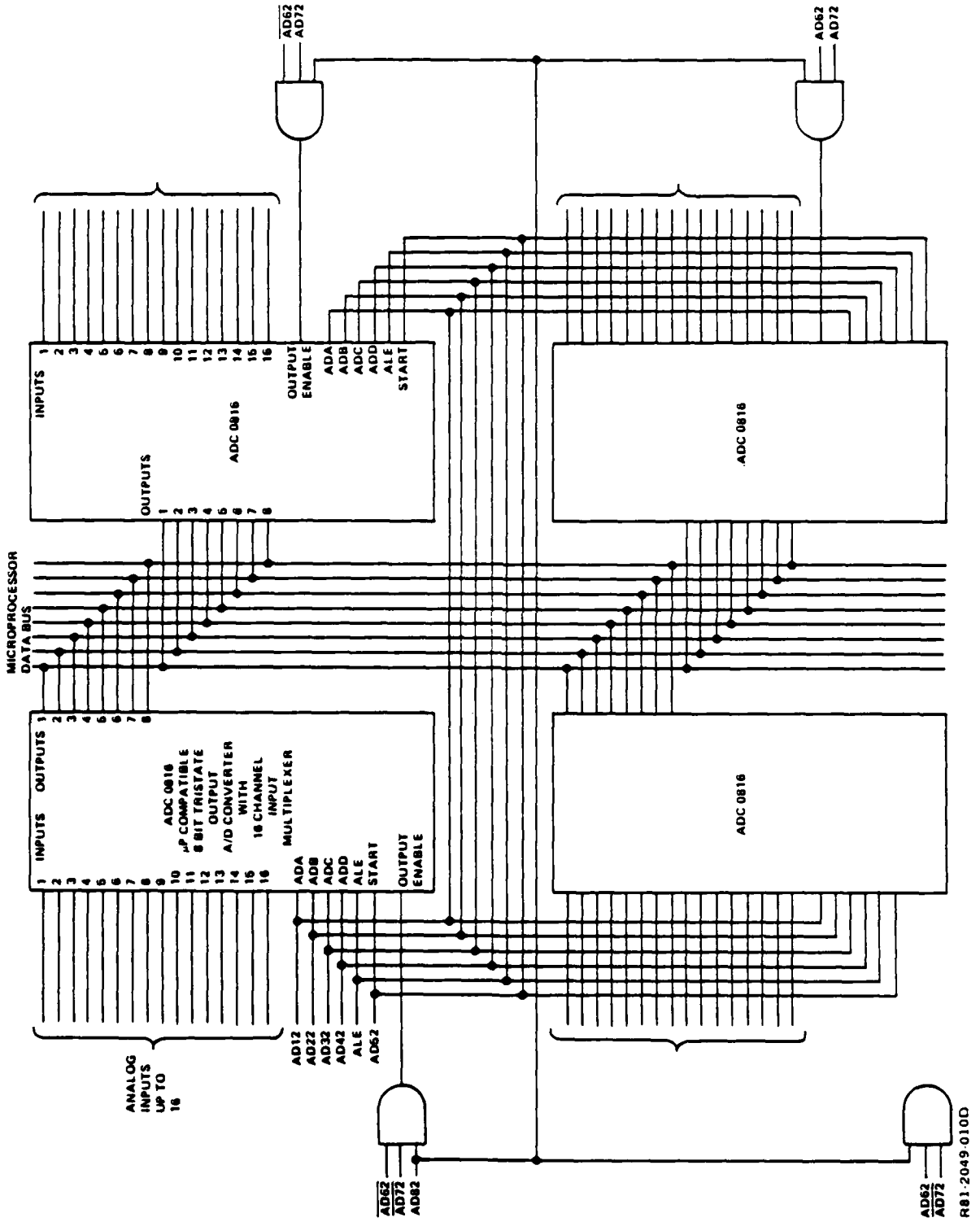

Fig. 3-5 Analog Multiplexer for 64 Analog Inputs

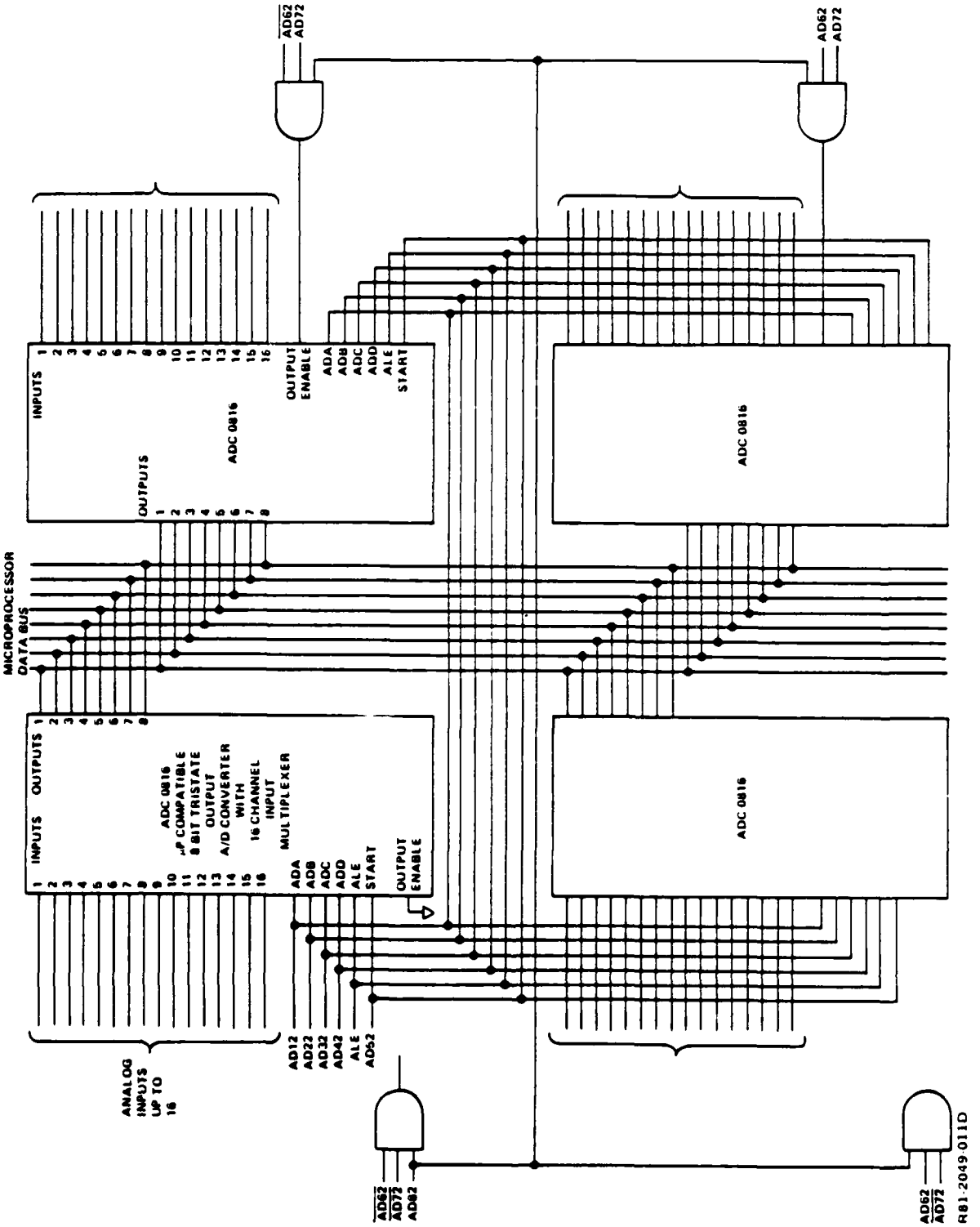

Fig. 3-6 Analog Multiplexer for 48 Additional Inputs

A typical operating sequence follows. A typical word out of the MP is 8 bits long and is expressed as a two-digit hexidecimal (H) number (see Table 3-1). The MP outputs word 00H through its number 2 port. Address bits AD62, AD72, and AD82 all being zero disables the outputs from the data bus; AD52 being zero does not allow the start of an A/D conversion; AD12, AD22, AD32, and AD42 being zero

TABLE 3-1 HEXADECIMAL NUMBERS

DECIMAL NUMBER	BINARY EQUIVALENT	HEXADECIMAL SYMBOL
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F

	PORT 2				ADDRESS OUTPUT			
	MORE SIGNIFICANT DIGIT				LESS SIGNIFICANT DIGIT			
ADDRESS:	AD7	A06	AD5	AD4	AD3	AD2	AD1	AD0
WEIGHT:	MSB			LSB	MSB			LSB
	X				Y			

WORD = X Y H

WHERE H MEANS HEXADECIMAL

X AND Y ARE HEXADECIMAL SYMBOLS.

EXAMPLES: 56H = 0101 0110 (BINARY) = 96 (DECIMAL)

FFH = 1111 1111 (BINARY) = 255 (DECIMAL)

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selects multiplexer position 0 on each ADC 0816 (latched into the device by the ALE signal from the MP).

The MP outputs word 10H through port number 2. This starts the A/D conversion on all the devices. After conversion is completed, the MP outputs word number 20H; no change in the address, no start conversion, AD82 = 0, AD72 = 0, AD62 = 1. Device number 1 has its output enabled and its data is loaded onto the data bus.

The MP inputs the data bus data, operates on it, increments positions 82, 72, and 62, and outputs the next word 40H, etc., until all the 7 ADC0816s have their address position '0' read.

The sequence is repeated for multiplexer addresses 1 through 15 (i.e., output 01H, 11H, 21H, input data bus, etc). The program performs 16 A/D conversions in each of the seven ADC0816 devices for a total of 112 analog inputs.

3.8 DISCRETE INPUTS AND DIGITAL INPUTS SCHEMATICS

The operation of the multiplexer schematic for 64 discrete inputs or 64 digital inputs are shown in Fig. 3-7.

All of the LS151 multiplexers are enabled to accept the same input number by addresses AD13, AD23, and AD33, but only one of the eight is enabled to the LS251 by addresses AD43, AD53, and AD63. The tri-state output of the LS251 is enabled by address AD73.

By using additional identical circuits, the multiplexing capability can be increased. The digital capacity can be expanded to 8 x 64 digital inputs by MP software.

3.9 ALPHANUMERIC DISPLAYS

A study of alphanumeric displays was made using the following groundrules:

- No CRT displays (large size, glass, high voltage, high power, lots of peripheral circuitry)

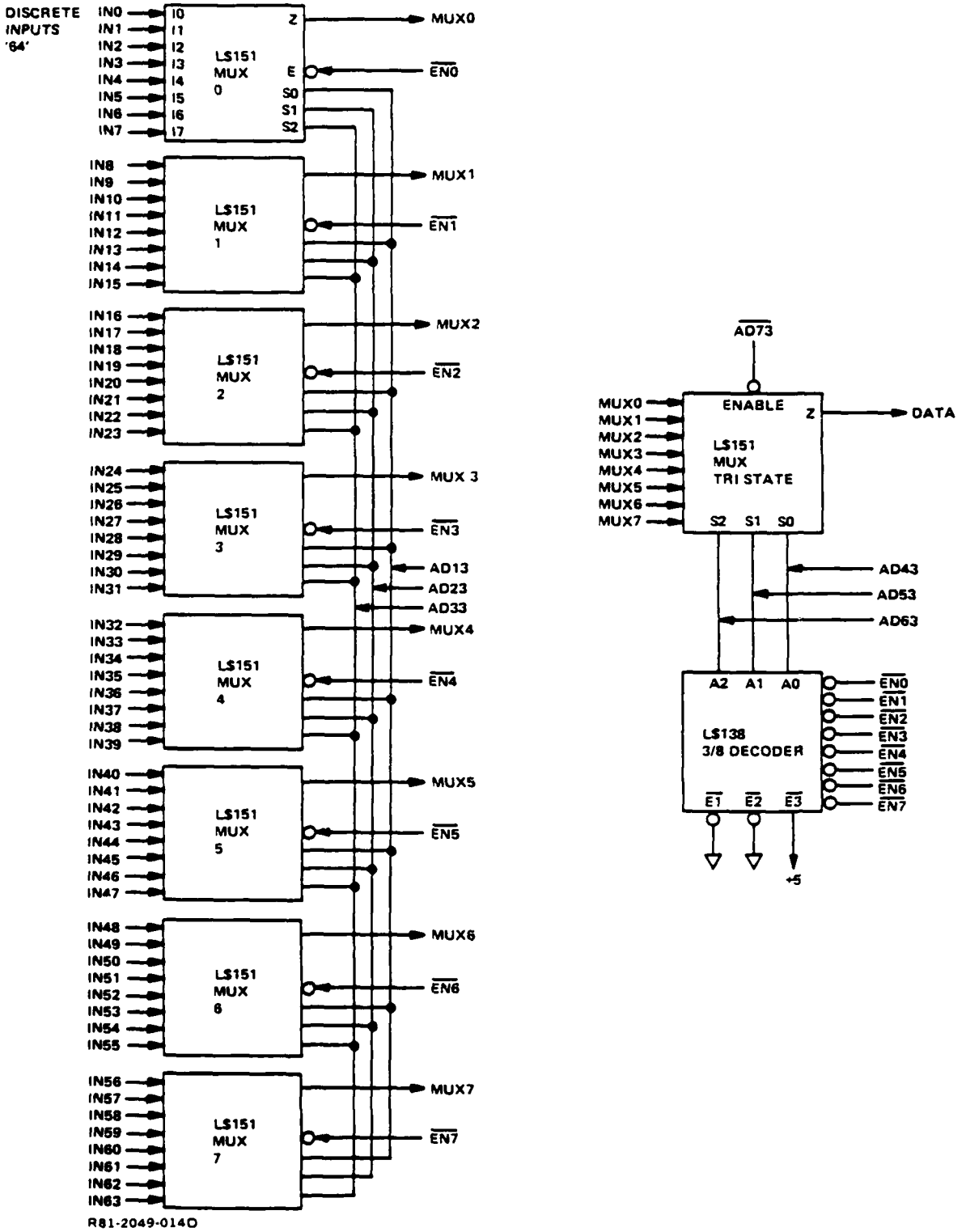

Fig. 3-7 Multiplexer Schematic for 64 Discrete or Digital Inputs

- The complete alphabet (eliminates seven and nine segment displays)
- Minimum heat dissipation (very difficult to remove heat from front panels)
- High light output (possible sunlight viewable)
- Rugged (shock and vibration)
- Long Life (avoid replacements)
- Capable of being multiplexed (minimum number of wires).

A listing of the companies contacted and their technology is shown in Table 3-2, Alphanumeric Display Sources.

3.9.1 Display Technologies

The following display technologies have been investigated:

1. Light Emitting Diode (LED). A solid-state device usually made up of GaAsP (galium arsenic phosphide) or GaP (galium phosphide). Light is emitted when current passes through the device in the forward direction. LEDs offer the advantages of low cost, direct drive from bipolar logic levels of 5 V, ruggedness, military temperature range of -55° to +100°C, ease of multiplexing, and a life in excess of 250,000 hr. Disadvantage are the high currents required for high brightness and limited color variety (colors available include red, green, yellow, and orange).
2. Liquid Crystal Displays (LCDs). Consist of a liquid crystal solution sandwiched between two glass plates that have segments etched on them. When the liquid crystals are excited by an electric field their molecules line up and reflect light. LCD advantages are low power consumption and good contrast ratio (sunlight viewable). Disadvantages include slow response time, not visible in poor or nonexistent lighting conditions, limited temperature operation (0°C to 55°C) and fragility (glass). Colors available are black, silver, amber, blue, gold, and purple.

TABLE 3-2 ALPHANUMERIC DISPLAY SOURCES

MANUFACTURER	INCANDESCENT	PLASMA GAS DISCHARGE	LED	LCD	VACUUM FLUORESCENT	ELECTRO-LUMINESCENT
AIRMAC TECH. SYSTEMS	✓					
AMERICAN ELECTRONIC LABS			✓			
AMPEREX				✓		
AND			✓	✓		
BECKMAN		✓		✓		
BURROUGHS		✓				
CHEMETRICS					✓	
CHERRY		✓				
CRYSTALOID				✓		
DAKTRONICS	✓		✓			
DALE		✓				
DAY-LIGHT	✓					
DIALIGHT	✓		✓			
DIGITAL COMPONENTS			✓	✓		
EAO SWITCH			✓			
ELECTRO PLASMA		✓				
EPSON				✓		
ESSCO IND.	✓	✓	✓	✓		
FAIRCHILD			✓	✓		
FERRANTIC					✓	
FUJITSU	✓					
GENERAL DIGITAL	✓					
GENERAL INSTRUMENT		✓				
HAMLIN			✓			
HEWLETT-PACKARD		✓				
HYCOM						✓
INFO-LITE	✓		✓			
IEE	✓	✓	✓	✓	✓	
INTER MARKET	✓		✓			
KOLLSMAN						✓
LADCOR				✓		
LIQUID XTAL DISPLAYS				✓		
LITRONIX			✓			
MASTER SPECIALTIES	✓		✓			
NATIONAL ELECTRONICS		✓				
NATIONAL SEMICONDUCTOR			✓			
NEC					✓	
NORDEN		✓				
NORITAKE					✓	
OPCOCA			✓		✓	
PAN AMERICAN TRADE DEV.	✓		✓	✓	✓	
PORTESCUP AVIONICS	✓					
REFAC ELECTRONICS	✓		✓	✓		
SEIKO				✓		
SHELLY			✓	✓		
TEC			✓			
TI			✓			
XCITRON			✓			
WAGNER	✓					
WAMCO	✓					

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3. Incandescent Displays. These are the oldest readouts and emit light by heating a filament to incandescence. Incandescents are directly viewed filament displays and can operate from 5-V levels. Operating temperature is -55°C to +100°C, adding filters makes additional colors available, and their lifetime is 60,000 to 100,000 hr (greatly affected by the temperature of the filament, which is a function of the operating voltage). Problems include high power drain and, because they are vacuum tubes, breakage.
4. Vacuum Flourescent Displays. Consist of a triode vacuum tube having a filament, a control grid, and a segmented anode coated with a flourescent phosphur. With a positive anode voltage, the phosphur glows when the grid goes positive and turns off when the grid becomes negative. A major advantage is their blue-green light output, which peaks near the center of the eye's spectral response and is less fatiguing than red or red-orange displays. Additional advantages are low power dissipation and a temperature range of -55°C to 100°C. Disadvantages are the continuous filament power drain, a life under 20,000 hr, and susceptibility to damage from shock.
5. Plasma Gas-Discharge Displays. Employ a helium-neon mixture that becomes ionized and glows in response to an applied DC voltage. "Nixie" tubes were the first of the gas discharge type devices to reach the display market. They draw low currents and have a life of about 150,000 hr; but they require high voltages for breakdown (170 to 200 V), temperature range is -20°C to +70°C, and they are glass and therefore subject to shock and vibration. Display is an orange color.
6. AC Thin-Film Electro-Luminescent (TFEL) Displays. Electro-luminescent powders are deposited on a thin-film substrate. This is a new technology with expectations of good temperature range (-55°C to +125°C), low

power, high brightness and luminous efficiency, and the ability to withstand shock and high altitudes. TFEL display development is being supported by the Army. Colors are yellow/orange and amber. They will be investigated further.

3.9.2 Methods of Displaying Alphanumerics

1. 5x7 Dot Matrix. Each character is composed of five columns of seven rows of dots (see Fig. 3-8). A typical font for a 128-character ASCII set is shown in Fig. 3-9. Note that upper and lower case alphabets are available, as are many special symbols.
2. 14-Line and 16-Line Segments. Each character is made up line segments as shown in Fig. 3-10. The difference between the 14- and 16-segment displays are in the top and bottom segments. Note that, in the 16-segment display, the A and D segments are split in half as compared to the 14-segment display. An example of the character set for a 14-segment alphanumeric display is shown in Fig. 3-11. An example of a 16-segment display is shown in Fig. 3-12. A typical placement of the decimal point (DP) and the top half of the colon (CO) are also shown. A variation on these displays involve skewing the lines and dots such that the top of the character is to the right of the bottom character. See Fig. 3-13 for an example of a skewed 16-segment display.

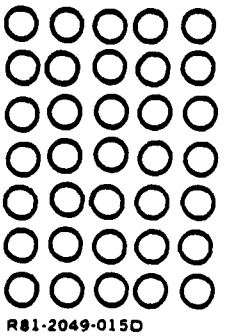

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Fig. 3-8 5 x 7 Dot Matrix

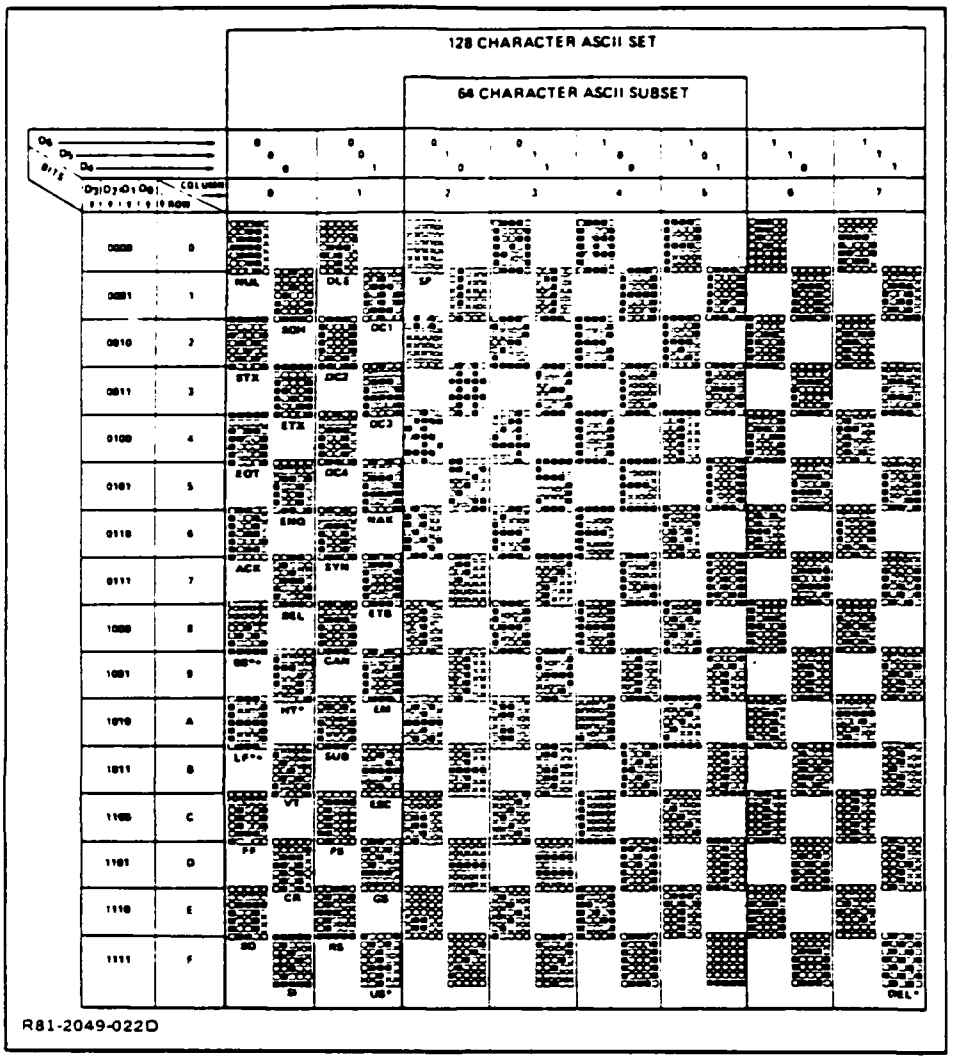


Fig. 3-9 Typical 128-Character Font

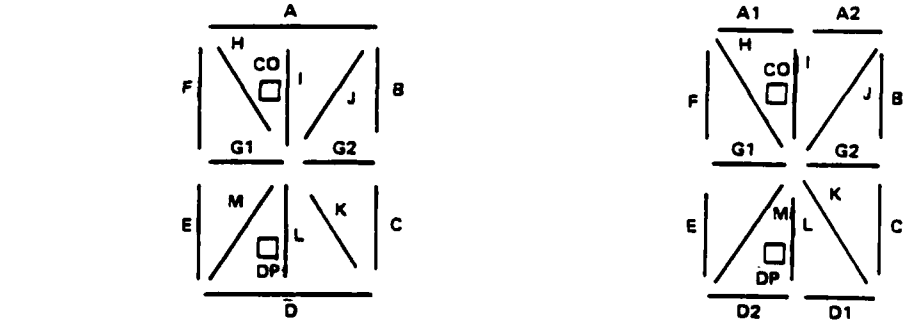
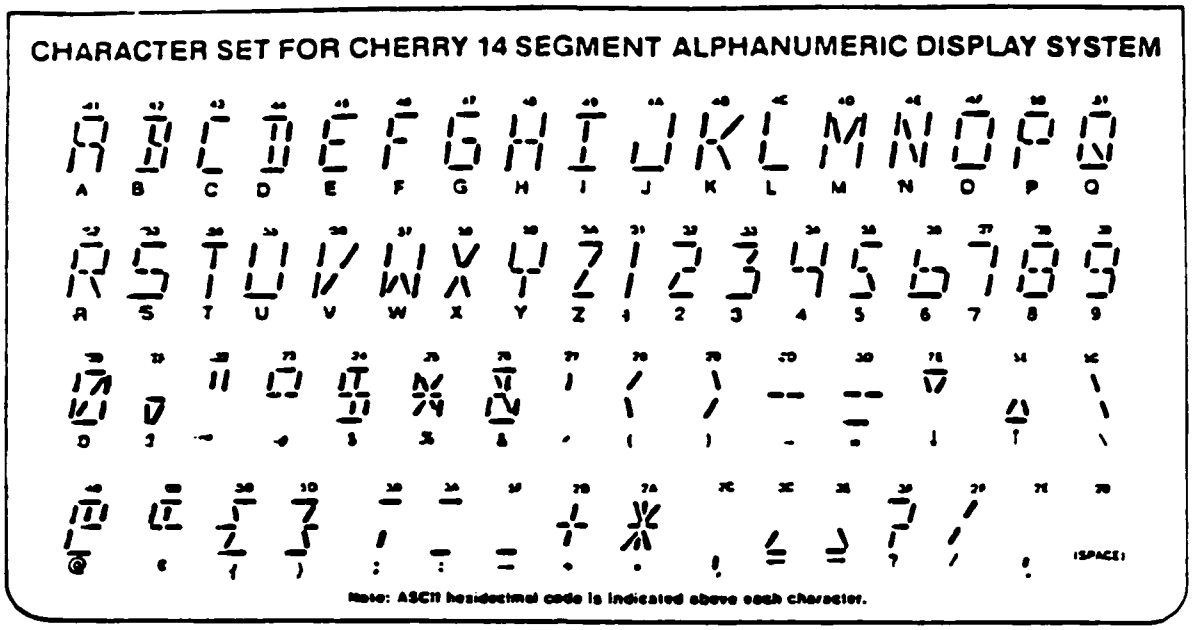


Fig. 3-10 Line Segments



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3-11 14-Line Segment Font

CHARACTER SET

D6 D5 D4 D3	D0 L	H	D1 L	H	D2 L	H	L	H
L H L L		!	"	#	$	%	&	'
L H L H	(	)	*	+	,	-	.	/
L H H L	0	1	2	3	4	5	6	7
L H H H	8	9	:	;	<	=	>	?
H L L L	@	A	B	C	D	E	F	G
H L L H	H	I	J	K	L	M	N	O
H L H L	P	Q	R	S	T	U	V	W
H L H H	X	Y	Z	[	\	]	^	_

All Other Input Codes Display "Blank"

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Fig. 3-12 16-Line Segment Font

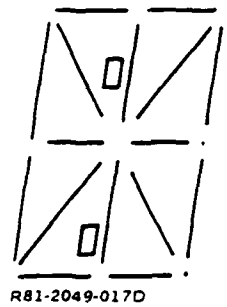

Fig. 3-13 Skewed 16-Segment Display

3.10 MEMORY

The 8751 microprocessor contains 4K bytes of PROM (4096 x 8 bits) for use as a program memory and 128 bytes of RAM (128 x 8 bits) to use for temporary storage.

A 2716-EPROM contains 2048 bytes (2048 x 8 bits) and will be used to store constants and limits. As the program sequences through the multiplexer, data from the sensors are sent to the microprocessor. These data are then compared to stored constants or limits for that sensor. The memory chip is a plug-in device and is different for various aircraft types (F-14, A-6, E-2, etc). One device is used for each system.

The 2764 EPROM contains 8192 bytes (8192 x 8 bits) and will be used to store failure messages for use in the display mode. Each message will consist of three 32-character sentences with enough information to identify the problem and the fix. For instance, a typical message can be:

HYDRAULIC FILTER #7 CLOGGED

FILTER IN ENGINE COMPARTMENT

REPLACE WITH PART # CC-07634

Using 96 eight-bit characters, one 2764 EPROM can store 85 messages. Using two of these devices allows 170 unique communications to be used per aircraft. These memory chips are plug-in devices and are unique to each aircraft type.

The X2201-30 NOVRAM is a 1024 x 1 bit nonvolatile RAM. Each of its 1024 positions can be used to store the fact that an error has or has not occurred. While the aircraft is in flight, one piece of data is inputted to the microprocessor and compared to a known value; if a failure is indicated, a "1" is stored in that bit position of the NOVRAM (a "0" is stored if there is no failure). When the HUDPS is being interrogated on the ground, the NOVRAM positions are sampled for a failure. Each of these positions has a unique error message associated with it (see 2764 above). One NOVRAM is required per aircraft and is permanently mounted.

Avoiding the use of batteries as a backup power source for solid-state read-write memories leads to using such devices as bubble memories or electrically eraseable/programmable read-only memories.

Bubble memories utilize magnetic bubble technology and require many additional IC components to control and load data into the bubble memory device. As of this writing Rockwell, TI, and National Semiconductor have dropped out of the bubble memory field, leaving Intel as the only American manufacturer. Intel's device can store one megabit by sequential access data in a 20-pin package that is 1.7 in. square by 0.43 in. thick. Maximum temperature range is 0°C to 70°C, with a complete system requiring +5 V and +12 V and approximately 32 W per ½ megabyte. The system is currently quite expensive (about $10,000).

Electrically eraseable read-only memories come in many acronyms from various manufacturers. These include EEPROM, EAROM, WAROM, and NOVRAM:

- Electrically Eraseable Programmable Read-Only Memory. Manufacturers include Hughes, Intel, and Motorola
- Electrically Alterable Read-Only Memory. Manufacturers include General Instrument and NCR
- Word Alterable Read-Only Memory. Manufactured by NCR
- Nonvolatile Random-Access Memory. Manufactured by Xicor.

Electrically eraseable PROMs can be erased and written into without removing them from the electronic circuit. They have a data retention lifetime with no power applied of approximately 10 years, but it takes approximately 10 msec to erase and about the same time to write new data into any one position. Once the unit is loaded with data, the access time of any location is less than 1 μsec. The EEPROM, EAROM, and WAROM can be erased at individual address positions or bulk-erased. Data is entered one address location at a time; this can be very time-consuming.

The NOVRAM is a novel device that contains both an EEPROM and a static RAM (a read/write memory) on one substrate. Nonvolatile data can be stored in the EEPROM and, at the same time, independent data can be accessed in the RAM. At any time, data can be transferred back and forth between the RAM and EEPROM with store and array recall signals. The NOVRAM uses a single 5-V supply for any function; regular EEPROMS require a high voltage (17 to 25 V) for writing and erasing. The RAM has typical read and write times of 300 nanosec. The store cycle to bulk transfer data from RAM to EEPROM is 10 msec max. The array recall time to transfer data from EEPROM to RAM is 1 msec. Price is in the $20 range.

This is a new single-source device, but is recommended for achieving a nonvolatile memory.

3.11 POWER REQUIREMENTS

The display circuitry requires about 3 A at 5 V, while flight circuitry requires 750 MA at 5V.

To conserve power while in flight, a DC-to-DC converter having an efficiency of about 75% will be used. This will mean that the unit will dissipate approximately 5 W in flight. On the ground, it is recommended that a laboratory 5-V, 5A power supply cable be plugged into the unit.

The current drains versus the Integrated Circuits are shown in Table 3-3.

TABLE 3-3 CURRENTS VERSUS PARTS

IC (DISPLAY)	QTY	CURRENT (mA) PER DEVICE	TOTAL CURRENT (mA)	
			FLIGHT ONLY	GROUND ONLY
8751	1	150	150	150
2764	2	55	–	110
2708	1	150	150	–
2201-30	1	55	55	55
ADC0816	7	3	21	–
LS151	16	10	160	–
LS251	2	10	20	–
LS138	2	10	20	–
55114	3	50	150	–
MISC			24	185
DISPLAY	1	2500	–	2500
TOTAL			750	3000

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3.12 ELECTRICAL PARTS LIST

Table 3-4 itemizes a typical electrical parts list.

A description of special components used in the HUDPS with copies of the manufacturers data sheets follows. The devices are:

- 8751: Single-Chip 8-Bit Microcomputer
- HDSP: 5x7 Dot Matrix Alphanumeric Display System
- ADC0816: Single Chip Data Acquisition System
- 2764, 2716: Ultraviolet Erasable Programmable Read-only Memories
- X2201-30: 1024x1 Nonvolatile Static RAM
- AD537: Voltage-to-Frequency Converter
- 54LS151: Data Selector/Multiplexer
- 54LS251: Tri-state Output Data Selector/Multiplexer.

3.12.1 8751: Single-Chip 8-Bit Microcomputer

This single-chip, 40-pin, single-voltage microcomputer manufactured by Intel contains features found in many multichip computer systems. The mathematical instructions of multiply and divide save hundreds of program steps and therefore debugging, while the subtract and compare instructions which are so necessary but not available on most microcomputers are also preprogrammed.

TABLE 3-4 ELECTRICAL PARTS LIST

QTY	PART NO.	DESCRIPTION	NO. OF PINS
		INTEGRATED CIRCUITS	
1	8751	MICROPROCESSOR	40
2	2764	EPROM	28
1	2716	EPROM	24
1	2201-30	NOVRAM	18
7	ADC0816	8-BIT TRI-STATE OUTPUT A/D CONVERTER WITH 16 INPUT MULTIPLEXER	40
16	LS151	8-INPUT MULTIPLEXER	16
2	LS251	TRI-STATE 8-INPUT MULTIPLEXER	16
2	LS138	3 TO 8 DECORDER	16
3	LS311	TRIPLE 3 INPUT "AND"	14
3	55114	DUAL DIFFERENTIAL LINE DRIVERS	16
2	55470	DUAL DRIVERS	14
6	MISC	TTL GATES	14
1	LM140	5 VDC REGULATOR	TO 3 METAL CAN
		DISPLAY CIRCUITS	
1	HDSP2432	32-CHARACTER HD ALPHANUMERIC DISPLAY, HEWLETT PACKARD	6.4 x 2.3 IN. PC BOARD
1	HDSP2471	DISPLAY INTERFACE INCORPORATING 128-CHARACTER ASCII DECODER, HEWLETT PACKARD	6.4 x 2.3 IN. PC BOARD
		PRINTED CIRCUIT BOARDS AND PC BOARD CONNECTORS	
6		6.5 x 5 IN.	
6		GC825BU: 66-PIN BOARD CONNECTOR	
6		GC825BN: 66-PIN MATE	
		BULKHEAD CONNECTORS	
1		12-PIN OUTPUT	
2		3-PIN POWER	
2		100-PIN INPUT	
		MISC ELECTRICAL COMPONENTS	
50		0.1 mF 100-VOLT CAPACITORS	
6		15 mF 15-VOLT CAPACITORS	
1		28 VDC INPUT LINE FILTER	
1		40-W RESISTOR	
250		1/8-W 5% RESISTORS	
1		12 MHz CRYSTAL	
		CHASSIS	
		7 IN. WIDE x 6 IN. HIGH x 8 IN. DEEP	

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Additional features include four 8-bit ports for 32 I/O lines, two 16-bit timer/event counters, and external program memory expandable to 64K bytes. With a 12-MHz crystal, 58% of the instructions are executed in 1 μsec, 40% are executed in a 2 μsec, and multiply and divide require 4 μsec each.

Fig. 3-14 is a copy of the data sheet for the 8751 family of devices. The 8751 has a user programmable and ultraviolet erasable PROM.

8051 Architectural Specification and Functional Description PRELIMINARY

8031/8051/8751
SINGLE-COMPONENT 8-BIT MICROCOMPUTER

- 8031 - Control Oriented CPU With RAM and I/O
- 8051 - An 8031 With Factory Mask- Programmable ROM
- 8751 - An 8031 With User Programmable/Erasable EPROM

- 4K x 8 ROM/EPROM
- 128 x 8 RAM
- Four 8-Bit Ports, 32 I/O Lines
- Two 16-Bit Timer/Event Counters
- High-Performance Full-Duplex Serial Channel
- Boolean Processor
- Compatible with MCS-80™/MCS-85™ Peripherals
- External Memory Expandable to 128K
- MCS-48™ Architecture Enhanced with:
  - Non-Paged Jumps
  - Direct Addressing
  - Four 8-Register Banks
  - Stack Depth Up to 128-Bytes
  - Multiply, Divide, Subtract, Compare
- Most Instructions Execute in 1μs
- 4μs Multiply and Divide

The Intel® 8031/8051/8751 is a stand-alone, high-performance single-chip computer fabricated with Intel's highly-reliable +5 Volt, depletion-load, N-Channel, silicon-gate HMOS technology and packaged in a 40-pin DIP. It provides the hardware features, architectural enhancements and new instructions that are necessary to make it a powerful and cost effective controller for applications requiring up to 64K bytes of program memory and/or up to 64K bytes of data storage.

The 8051/8751 contains a non-volatile 4K x 8 read only program memory; a volatile 128 x 8 read/write data memory; 32 I/O lines; two 16-bit timer/counters; a five-source, two-priority-level, nested interrupt structure; a serial I/O port for either multi-processor communications, I/O expansion, or full duplex UART; and on-chip oscillator and clock circuits. The 8031 is identical, except that it lacks the program memory. For systems that require extra capability, the 8051 can be expanded using standard TTL compatible memories and the byte oriented MCS-80 and MCS-85 peripherals.

The 8051 microcomputer, like its 8048 predecessor, is efficient both as a controller and as an arithmetic processor. The 8051 has extensive facilities for binary and BCD arithmetic and excels in bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 12 MHz crystal, 58% of the instructions execute in 1μs, 40% in 2μs and multiply and divide require only 4μs. Among the many instructions added to the standard 8048 instruction set are multiply, divide, subtract and compare.

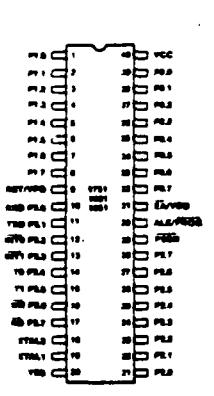


Figure 1. Pin Configuration

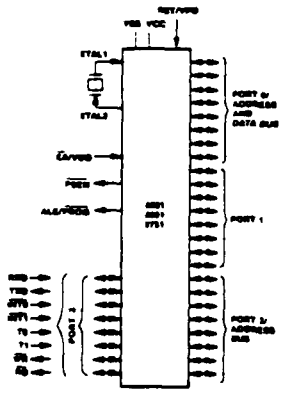


Figure 2. Logic Symbol

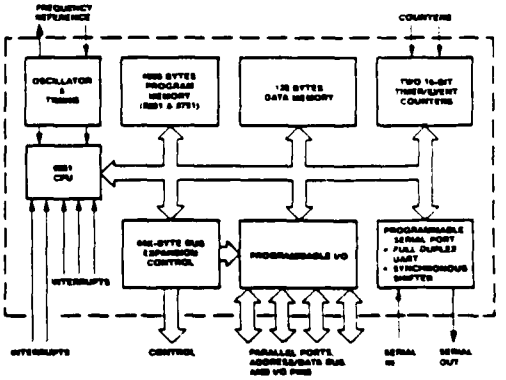


Figure 3. Block Diagram

AFN-01468A-02

R81-2049-020D

Fig. 3-14 Intel 8751 Data Sheet

3.12.2 HDSP: 5 x 7 Dot Matrix Alphanumeric Display System

A two-board system made by Hewlett-Packard has been studied as a possible smart display. The units chosen were the HDSP-2432 (a single-line, 32-character LED display panel) and the HDSP-2471 (display interface which incorporates a 128-character ASCII decoder). A copy of the data sheet is provided in Fig. 3-15.

The alphanumeric display controller consists of a preprogrammed microprocessor plus associated logic to provide decode, memory, and drive signals to interface the display panel to the user's system.

3.12.3 ADC0816: Single-Chip Data Acquisition System

This single 40-pin chip manufactured by National Semiconductor contains a 16-channel analog multiplexer controlled by a 4-bit address, an 8-bit analog-to-digital (A/D) converter with a conversion time of 100 μsec, and an 8-bit tri-state output latch buffer that allows the digital outputs to be tied to the microprocessor data bus under control of the microprocessor.

The 16-channel multiplexer allows seven integrated circuits to control 112 analog inputs using one 8-bit port from the microprocessor. Four bits select one of the 16 inputs on each unit, one bit is used to start the A/D conversion, and three bits select which of the seven chips (or none) is to be tied to the data bus.

A copy of a data sheet is given in Fig. 3-16 and includes a list of some additional features of the device, such as a single 5-V supply and a low-power (15 mW) requirement. The ADC0816CD is a ceramic device that has an operating temperature range of -55°C to +125°C.

3.12.4 2764: 8K x 8 Ultraviolet Erasable PROM

The 2764 is a 5-V only, 65,536-bit ultraviolet erasable programmable read-only memory (EPROM) in a single 28-pin integrated circuit. It is a nonvolatile memory that can be used to store the microprocessor program memory and the stored message for each input signal. This device can store 8192 8-bit characters which can be broken

HEWLETT PACKARD

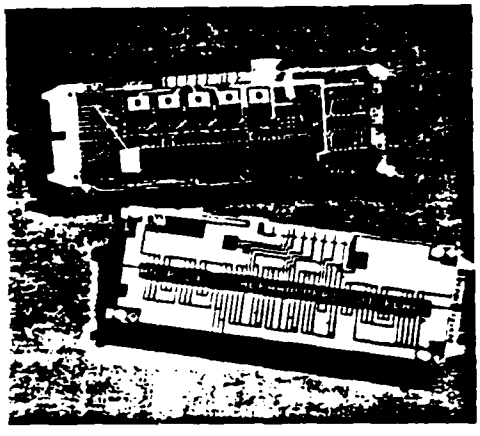
5 x 7 DOT MATRIX ALPHANUMERIC DISPLAY SYSTEM

HDSP - 2416
HDSP - 2424
HDSP - 2432
HDSP - 2440
HDSP - 2470
HDSP - 2471
HDSP - 2472

TECHNICAL DATA MARCH 1980

Features

- **COMPLETE ALPHANUMERIC DISPLAY SYSTEM UTILIZING THE HDSP-2000 DISPLAY**
- **CHOICE OF 64, 128, OR USER DEFINED ASCII CHARACTER SET**
- **CHOICE OF 16, 24, 32, or 40 ELEMENT DISPLAY PANEL**
- **MULTIPLE DATA ENTRY FORMATS — Left, Right, RAM, or Block Entry**
- **EDITING FEATURES THAT INCLUDE CURSOR, BACKSPACE, FORWARDSPACE, INSERT, DELETE, AND CLEAR**
- **DATA OUTPUT CAPABILITY**
- **SINGLE 5.0 VOLT POWER SUPPLY**
- **TTL COMPATIBLE**
- **EASILY INTERFACED TO A KEYBOARD OR A MICROPROCESSOR**



Description

The HDSP-24XX series of alphanumeric display systems provides the user with a completely supported 5 x 7 dot matrix display panel. These products free the user's system from display maintenance and minimize the interaction normally required for alphanumeric displays. Each alphanumeric display system is composed of two component parts:

1. An alphanumeric display controller which consists of a preprogrammed microprocessor plus associated logic, which provides decode, memory, and drive signals necessary to properly interface a user's system to an HDSP-2000 display. In addition to these basic display support operations, the controller accepts data in any of four data entry formats and incorporates several powerful editing routines.
2. A display panel which consists of HDSP-2000 displays matched for luminous intensity and mounted on a P C. board designed to have low thermal resistance.

These alphanumeric display systems are attractive for applications such as data entry terminals, instrumentation, electronic typewriters, and other products which require an easy to use 5 x 7 dot matrix alphanumeric display system.

PART NUMBER	DESCRIPTION
Display Boards	
HDSP-2416	Single-line 16 character display panel utilizing the HDSP-2000 display
HDSP-2424	Single-line 24 character display panel utilizing the HDSP-2000 display
HDSP-2432	Single-line 32 character display panel utilizing the HDSP-2000 display
HDSP-2440	Single-line 40 character display panel utilizing the HDSP-2000 display
Controller Boards	
HDSP-2470	HDSP-2000 display interface incorporating a 64 character ASCII decoder
HDSP-2471	HDSP-2000 display interface incorporating a 128 character ASCII decoder
HDSP-2472	HDSP-2000 display interface without ASCII decoder. Instead, a 24 pin socket is provided to accept a custom 128 character set from a user programmed 1K x 8 PROM.

When ordering, specify one each of the Controller Board and the Display Board for each complete system.

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Fig. 3-15 Hewlett-Packard 5 x 7 Dot Display System

National Semiconductor

Analog-to-Digital Converters

ADC0816, ADC0817 Single Chip Data Acquisition System

General Description

The ADC0816, ADC0817 (MM74C948) data acquisition components are monolithic CMOS devices with an 8-bit analog-to-digital converter, a 16-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 16-channel multiplexer can directly access any one of 16 single-ended analog signals and provides the logic for additional channel expansion. Signal conditioning of any analog input signal is eased by direct access to the input of the 8-bit A/D converter.

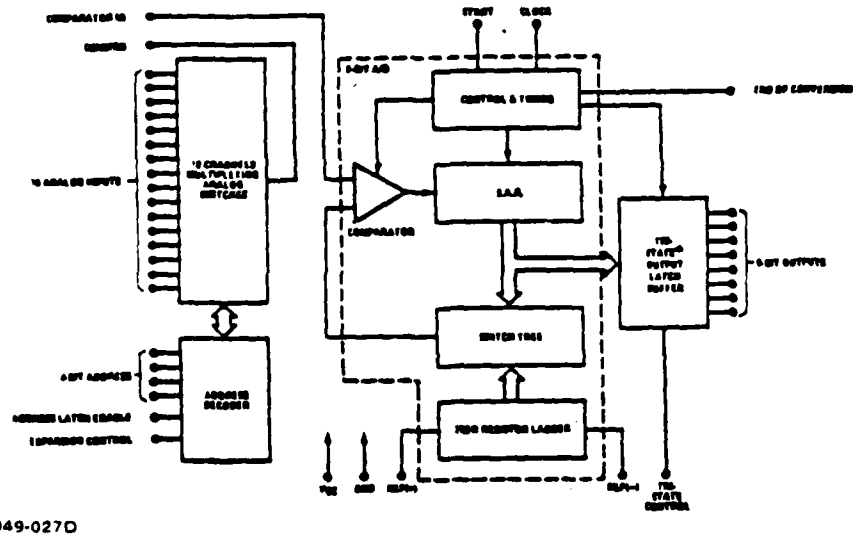
The device eliminates the need for external zero and full-scale adjustments and features an absolute accuracy ≤ 1 LSB including quantizing error. Easy interfacing to microprocessors is provided by the latched and decoded address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0816, ADC0817 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0816, ADC0817 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited for applications such as process control, industrial control, and machine control. For similar performance except 8-channel multiplexer in a 28-pin package, see ADC0808 data sheet.

Features

- Total unadjusted error < ±1/2 LSB
- Linearity error < ±1/2 LSB
- No missing codes
- Guaranteed monotonicity
- No offset adjust required
- No scale adjust required
- Conversion time of 100 µs
- Easy microprocessor interface
- Latched TRI-STATE output
- Latched address input
- Ratiometric conversion
- Single 5V supply
- Low power consumption—15 mW
- Full military temperature range available

Block Diagram



R81-2049-027D

Fig. 3-16 Single Chip Data Acquisition System

up into 85 messages, each 96 characters long. A copy of the data sheet is enclosed (Fig. 3-17).

3.12.5 2708, 2716, 2732: Ultraviolet EPROM

The 2708, 2716, and 2732 EPROMs are smaller (and cheaper) memory size devices that have 8192, 16384, and 32768-bit capacities, respectively. These smaller devices can be used to keep track of constants and to expand on the 2764 above.

3.12.6 X2201-30: 1024 x 1 Nonvolatile Static RAM

This 18-pin, single-voltage memory chip manufactured by Xicor contains two 1K memories mounted in a single integrated circuit. One memory is a 1K static RAM which is overlaid bit-for-bit with a 1K Electrically Erasable PROM (EEPROM). Data can be written into or read out of the RAM at speeds of 300 nanosec. Upon a command to store, data from the RAM are written into the EEPROM (required time of 10 msec).

Data will remain unchanged in the EEPROM with or without power supplied until the next store command. Upon power-up or an array recall command, data in the EEPROM are copied back into the RAM nondestructively. The data are now in RAM and EEPROM.

Fig. 3-18 is a copy of the data sheet.

3.12.7 AD537: Voltage-to-Frequency Converter

This single 14-pin monolithic integrated circuit manufactured by Analog Devices converts input analog signals to a constant-amplitude frequency which is linearly dependent on the input voltage according to the equation

$$F = \frac{V}{10RC},$$

Where R and C are external components; R is determined by the maximum input full scale voltage and C by the maximum desired output frequency.

The AD537 is linearly dependent on temperature and can be used directly as a temperature transducer scaled for Fahrenheit or Centigrade by selection of the external resistor and capacitor.

intel

PRELIMINARY

2764
(8K x 8) UV ERASABLE PROM

- 200 ns (2764-2) Maximum Access Time . . . HMOS*-E Technology
- Compatible to High Speed 8mHz 8086-2 MPU . . . Zero WAIT State
- Two Line Control
- Pin Compatible to 2732A EPROM
- Industry Standard Pinout . . . JEDEC Approved
- Low Active Current...100mA Max.

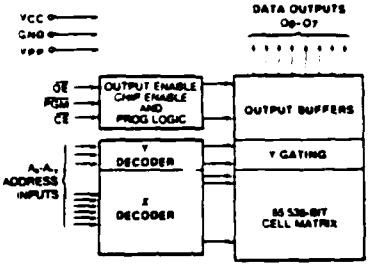
The Intel® 2764 is a 5V only, 65,536-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The standard 2764 access time is 250ns with speed selection available at 200ns. The access time is compatible to high performance microprocessors, such as Intel's 8mHz 8086-2. In these systems, the 2764 allows the microprocessor to operate without the addition of WAIT states.

An important 2764 feature is the separate output control, Output Enable ($\overline{OE}$) from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple bus microprocessor systems. Intel's Application Note AP-72 describes the microprocessor system implementation of the $\overline{OE}$ and $\overline{CE}$ controls on Intel's EPROMs. AP-72 is available from Intel's Literature Department.

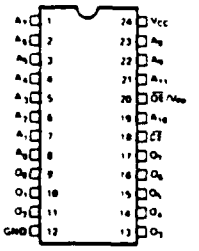
The 2764 has a standby mode which reduces the power dissipation without increasing access time. The active current is 100mA, while the standby current is only 50mA. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input.

The 2764 is fabricated with HMOS*-E technology, Intel's high-speed N-channel MOS Silicon Gate Technology.

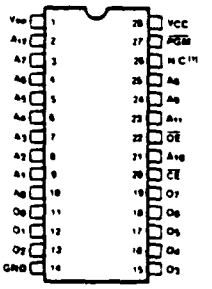
BLOCK DIAGRAM



2732A PIN CONFIGURATION



2764 PIN CONFIGURATION



(1) For total compatibility and upgradability from the 2732A and ROMs provide a trace to pin 26.

MODE SELECTION

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	X	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	High Z

X can be either V_{IL} or V_{IH}.

PIN NAMES

A_0-A_{12}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS
$\overline{PGM}$	PROGRAM
N.C.	NO CONNECT

*HMOS is a patented process of Intel Corporation.

December 1980
AFN-01647A

R81-2049-023D

Fig. 3-17 Single Chip Data Acquisition System

Characteristics Subject to Change

XICOR™

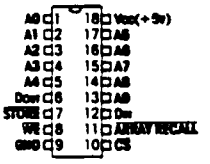
1024 x 1 Bit Nonvolatile Static RAM
Array Recall Feature

X2201-30

- **NONVOLATILE STATIC RAM:** The X2201 contains 2K bits of memory organized as a conventional 1K static RAM overlaid bit-for-bit with a nonvolatile 1K Electrically Erasable PROM (E^2PROM). Nonvolatile data can be stored in the E^2PROM and at the same time independent data can be accessed in the RAM memory. At any time, data can be transferred back-and-forth between the RAM and E^2PROM by simple store and array recall signals.
- **5V ONLY:** High-voltage pulses or supplies are never required. A single 5V supply is the *only power source* ever required for any function.
- **EASE-OF-USE:** Unprecedented simplicity, all inputs and outputs are directly TTL compatible. Fully static timing. Three-state output. 18-pin package.
- **PERFORMANCE:** RAM cycle time is less than 300 ns. During the lifetime of the device, data can be recalled from the E^2PROM an unlimited number of times.
- **POWER-FAILURE PROTECTION:** One simple TTL signal saves the entire RAM database. A snapshot nonvolatile copy of all RAM data is internally stored safe without power and can be recalled to the RAM when power returns. No battery backup required.

Xicor's X2201 is fabricated with reliable n-channel floating gate MOS technology. For systems where RAM nonvolatility or *in-the-circuit* ROM changes by TTL signals are important, the Xicor X2201 featuring array recall is the ideal choice.

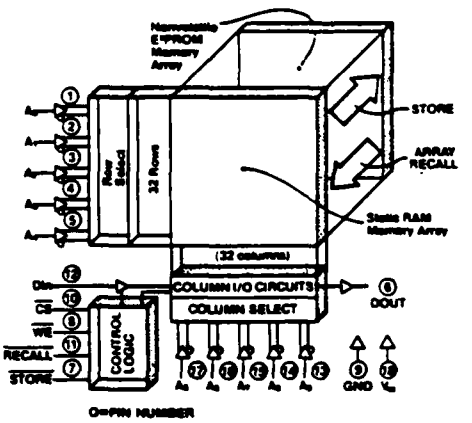
PIN CONFIGURATION
18 PIN DIP .300"



PIN NAMES

A_0–A_9	ADDRESS INPUTS
D_{IN}	DATA INPUT
D_{OUT}	DATA OUT
$\overline{WE}$	WRITE ENABLE
$\overline{CS}$	CHIP SELECT
$\overline{ARRAY\ RECALL}$	ARRAY RECALL
$\overline{STORE}$	STORE
V_{CC}	+5V
GND	GROUND

FUNCTIONAL DIAGRAM



TRUTH TABLE

INPUTS					OUTPUT	
$\overline{CS}$	$\overline{WE}$	D_{IN}	ARRAY RECALL	STORE	D_{OUT}	MODE
H	X	X	X	X	High Z	Not Selected (1), (2)
L	L	L	H	H	High Z	Write "0" RAM
L	L	H	H	H	High Z	Write "1" RAM
L	H	X	L	H	High Z	Array Recall
L	H	X	H	L	High Z	Nonvolatile Storing (2)
L	H	X	H	H	D_{OUT}	Reading RAM

NOTES: (1) Chip is deselected but may be automatically completing a store cycle.
(2) $\overline{CS}$ = L and $\overline{STORE}$ = L are required only to initiate the store cycle, after which the store cycle will be automatically completed ($\overline{CS}$ = X and $\overline{STORE}$ = X).

Data sheet effective April 1980 Revision C

XICOR, INC., 1221 Innsbruck Drive, Sunnyvale, California 94086 Telephone: (408) 734-3041 TWX: 910-379-0033

R81-2049-024D

Fig. 3-18 Non-volatile Static RAM Data Sheet

The frequency signal is inputted to a counter for a unit time determined by the microprocessor to become a useable digital number.

Fig. 3-19 is a copy of the data sheet for the device.

3.12.8 54LS151: Data Selector/Multiplexer

This single-chip, 16-pin device accepts eight digital inputs and selects one of these as an output by decoding a 3-input data select from the MP. This device operates from a single 5-V supply and has a typical power dissipation of 30 mW. A copy of the data sheet is shown in Fig. 3-20.

3.12.9 54LS251: Tri-State Data Selector/Multiplexer

This single-chip, 16-pin device operates identically to the 54LS151 with the exception that it can have a tri-state output, making it ideal for driving a data bus. This unit operates from a single 5-V supply and has a typical power dissipation of 35 mW. A copy of the data sheet is shown in Fig. 3-21.

ANALOG DEVICES

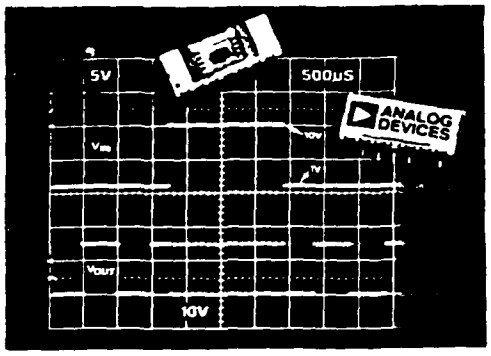
Integrated Circuit Voltage to Frequency Converter

AD537

PRELIMINARY TECHNICAL DATA

FEATURES

- Low Cost A-D Conversion
- Versatile Input Amplifier
  - Positive or Negative Voltage Modes
  - Negative Current Mode
  - High Input Impedance, Low Drift
- Single Supply, 5 to 36 Volts
- Linearity: ±0.05%
- Low Power: 1.2mA Quiescent Current
- Full Scale Frequency up to 100kHz
- 1.00 Volt Reference
- Thermometer Output (1mV/°K)
- F-V Applications



PRODUCT DESCRIPTION

The AD537 is a monolithic V-F converter consisting of an input amplifier, a precision oscillator system, an accurate internal reference generator and a high current output stage. Only a single RC network is required externally to set up any full scale (F.S.) frequency up to 100kHz and any F.S. input voltage up to +30V. Linearity error is as low as ±0.05% for 10kHz F.S. and operation is guaranteed over an 80dB dynamic range. The converter performs very well even at very low frequencies, maintaining linearity down to 0.001Hz; accuracy at this level is limited only by input offset voltage and current. The overall temperature coefficient (excluding the effects of external components) is typically ±30ppm/°C. The AD537 operates from a single supply of 5 to 36V and consumes only 1.2mA quiescent current.

A temperature-proportional output, scaled to 1.00mV/°K, enables the circuit to be used as a reliable temperature-to-frequency converter; in combination with the fixed reference output of 1.00V, scales down to 0°C or 0°F can be generated.

The low drift (1µV/°C typ) input amplifier allows operation directly from small signals (e.g. thermocouples or strain gauges) while offering a high (250MΩ) input resistance. Unlike most V-F converters, the AD537 provides a square-wave output, and can drive up to 12 TTL loads, LEDs, very long cables, etc.

The excellent temperature characteristics and long-term stability of the AD537 are guaranteed by the primary band-gap reference generator and the low T.C. silicon chromium thin film resistors used throughout.

The circuit is available in a hermetically-sealed 14 pin DIL package and in three grades: the AD537J and K for 0 to +70°C operation and the AD537S, specified from -55 to +125°C.

PRODUCT HIGHLIGHTS

1. The AD537 is a complete V-F converter requiring only an external RC timing network to set the desired full scale frequency and a selectable pull-up resistor for the open-collector output stage. Any full-scale input voltage range from 100mV to 10 volts (or greater, depending on $+V_S$) can be accommodated by proper selection of timing resistor. The full scale frequency is then set by the timing capacitor from the simple relationship, f = V/10RC.
2. The power supply requirements are minimal, only 1.2mA quiescent current is drawn from a single positive supply from 4.5 to 36 volts. In this mode, positive inputs can vary from 0 volts (ground) to ($+V_S$ - 4) volts. Negative inputs can easily be connected for below ground operation.
3. F-V converters with excellent characteristics are also easy to build by connecting the AD537 in a phase-lock loop, application particulars are shown on page 6.
4. The versatile open-collector NPN output stage can sink up to 20mA with a saturation voltage less than 0.4 volts. The Logic Common terminal can be connected to any level between ground (or $-V_S$) and 4 volts below $+V_S$. This allows easy direct interface to any logic form with either positive or negative logic levels.
5. Every AD537 is subjected to long term stabilization bakes and temperature cycled 10 times from -65 to +150°C prior to final test to insure reliability and long-term stability.

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Fig. 3-19 Voltage to Frequency Converter Data Sheet

TYPES SN54150, SN54151A, SN54152A, SN54LS151, SN54LS152, SN54S151, SN74150, SN74151A, SN74LS151, SN74S151
DATA SELECTORS/MULTIPLEXERS

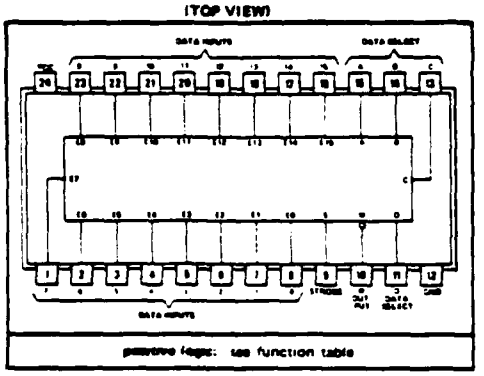
BULLETIN NO. DL-S 7611819, DECEMBER 1972–REVISED OCTOBER 1976

- '150 Selects One-of-Sixteen Data Sources
- Others Select One-of-Eight Data Sources
- Performs Parallel-to-Serial Conversion
- Permits Multiplexing from N Lines to One Line
- Also For Use as Boolean Function Generator
- Input-Clamping Diodes Simplify System Design
- Fully Compatible with Most TTL and DTL Circuits

TYPE	TYPICAL AVERAGE PROPAGATION DELAY TIME DATA INPUT TO W OUTPUT	TYPICAL POWER DISSIPATION
'150	11 ns	200 mW
'151A	8 ns	145 mW
'152A	8 ns	130 mW
'LS151	11 ns†	30 mW
'LS152	11 ns†	28 mW
'S151	4.5 ns	225 mW

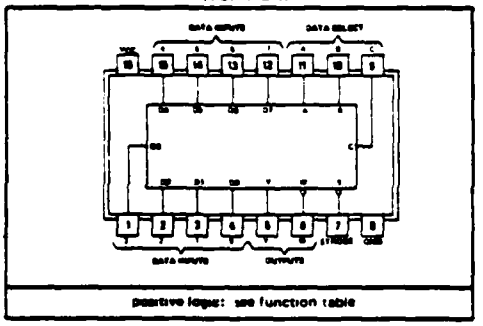
† Typical data

SN54150 . . . J OR W PACKAGE
SN74150 . . . J OR N PACKAGE
(TOP VIEW)



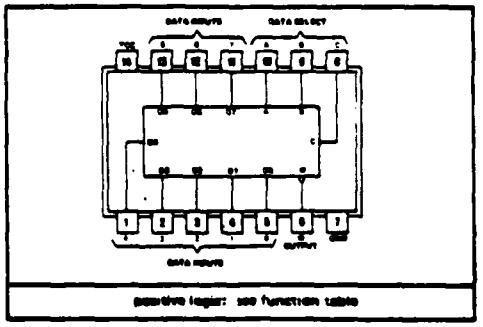
positive logic: see function table

SN54151A, SN54LS151, SN54S151 . . . J OR W PACKAGE
SN74151A SN74LS151, SN74S151 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

SN54152A, SN54LS152 . . . W PACKAGE
(TOP VIEW)



positive logic: see function table

description

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select the desired data source. The '150 selects one-of-sixteen data sources; the '151A, '152A, 'LS151, 'LS152, and 'S151 select one-of-eight data sources. The '150, '151A, 'LS151, and 'S151 have a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the W output high, and the Y output (as applicable) low.

The '151A, 'LS151, and 'S151 feature complementary W and Y outputs whereas the '150, '152A, and 'LS152 have an inverted (W) output only.

The '151A and '152A incorporate address buffers which have symmetrical propagation delay times through the complementary paths. This reduces the possibility of transients occurring at the output(s) due to changes made at the select inputs, even when the '151A outputs are enabled (i.e., strobe low).

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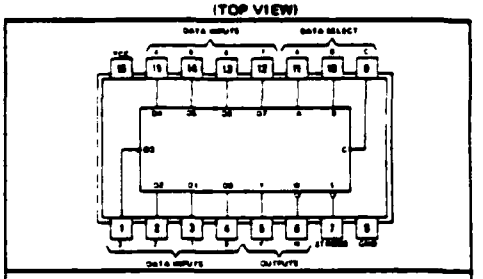
Fig. 3-20 Data Selector/Multiplexer Data Sheet

TTL
MSI

TYPES SN54251, SN54LS251, SN54S251, SN74251, SN74LS251 (TIM9905), SN74S251 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7611834, DECEMBER 1972—REVISED OCTOBER 1976

SN54251, SN54LS251, SN54S251 . . . J OR W PACKAGE
SN74251, SN74LS251, SN74S251 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

- Three-State Versions of '151, 'LS151, 'S151
- Three-State Outputs Interface Directly with System Bus
- Perform Parallel-to-Serial Conversion
- Permit Multiplexing from N-lines to One Line
- Complementary Outputs Provide True and Inverted Data
- Fully Compatible with Most TTL and DTL Circuits

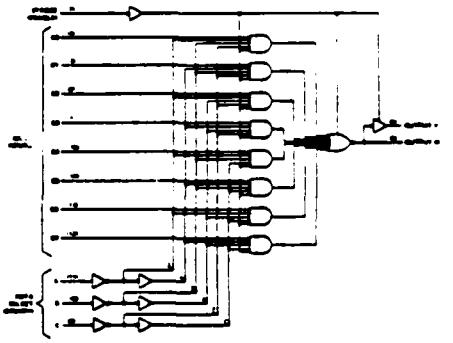
TYPE	MAX NO. OF COMMON OUTPUTS	TYPICAL AVG PROP DELAY TIME (D TO Y)	TYPICAL POWER DISSIPATION
SN54251	49	17 ns	250 mW
SN74251	129	17 ns	250 mW
SN54LS251	49	17 ns	35 mW
SN74LS251	129	17 ns	35 mW
SN54S251	39	8 ns	275 mW
SN74S251	129	8 ns	275 mW

description

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources and feature a strobe-controlled three-state output. The strobe must be at a low logic level to enable these devices. The three-state outputs permit a number of outputs to be connected to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the 'average output disable time is shorter than the average output enable time. The SN54251 and SN74251 have output clamp diodes to attenuate reflections on the bus line.

functional block diagram



FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	S		
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high logic level, L = low logic level
X = irrelevant, Z = high impedance (off)
D0, D1 . . . D7 = the level of the respective D input

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R81-2049-029D

Fig. 3-21 Tri-State Data Selector/Multiplexer

4 - CONCLUSIONS AND RECOMMENDATIONS

4.1 CONCLUSIONS

This six-month study contract validated the concept that a Hydraulic Diagnostic System (Display/processor) could be designed for universal application by any Navy aircraft.

A rapid change in software would compensate for Hydraulics System differences and variation in sensor requirements.

The display panel, driven by its own microprocessor circuit, is universal for all intended vehicles.

A nonvolatile memory approach permits storage of flight sensor information even after shutdown and without the use of batteries.

4.2 RECOMMENDATIONS

Based on the results of this study, the following recommendations are proposed.

- Continue with a design development study for the F-14A/A-6E vehicle
- Establish the common type of sensors required for each vehicle with their respective limits and output parameters
- Manufacture three shipsets, systems for testing on the F-14 a hydraulic simulator, A-6E flight test vehicle, and possibly the E-2C pending Navy authorization.

5 - REFERENCES

1. Proposed AIR xxx Aircraft Hydraulic System Characteristics.

2. NADC Report No. TR75160-30 "Final Engineering Report - Phase I HYCOS".

3. NADC Interim Report No. TR76309-30 "Hydraulic Diagnostic Monitoring System".

4. NADC Report No. TR76390-30 "Hydraulic Diagnostic Monitoring System".

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